EXHIBIT 1

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Paper 42
Entered: December 10, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2023-00847
Patent 10,268,608 B2

Before JON M. JURGOVAN, SHEILA F. McSHANE, and KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

McSHANE, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claims Unpatentable
Dismissing Petitioner's Motion to Exclude
Dismissing Patent Owner's Motion to Submit Supplemental Information
Granting-in-Part and Denying-in-Part Patent Owner's Motion to Strike
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background

Samsung Electronics Co., Inc. ("Petitioner") filed a Petition (Paper 1, "Pet.") requesting *inter partes* review of claims 1–12 (the "challenged claims") of U.S. Patent No. 10,268,608 B2 (Ex. 1001, "the '608 patent"), along with the Declaration of Dr. Robert Wedig (Ex. 1003). Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 6, "Prelim. Resp."). In the Preliminary Response, Patent Owner indicated that it filed a statutory disclaimer disclaiming claims 6–12 of the '608 patent. Prelim. Resp. 2–3 (citing Ex. 2001). With authorization, Petitioner filed a Reply to the Preliminary Response (Paper 9), and Patent Owner filed a Sur-reply to the Reply to the Preliminary Response (Paper 10).

On December 12, 2023, the Board instituted an *inter partes* review of the challenged claims pursuant to 35 U.S.C. § 314. Paper 13 ("Dec.").

After institution, Patent Owner filed a Patent Owner Response (Paper 20, "PO Resp."), along with the Declaration of Dr. William Henry Mangione-Smith (Ex. 2013). Petitioner filed a Reply (Paper 23, "Pet. Reply") and Patent Owner filed a Sur-reply (Paper 29, "PO Sur-reply").

Petitioner filed a Motion to Exclude (Paper 31), with Patent Owner filing an Opposition (Paper 36), and Petitioner filing a Reply to the Opposition (Paper 38). Patent Owner filed a Motion to Strike (Paper 25), with Petitioner filing an Opposition (Paper 27). Patent Owner filed a Motion to File Supplemental Information (Paper 35), with Petitioner filing an Opposition (Paper 37). The parties then presented oral arguments at a hearing on September 5, 2024, and a transcript of it has been entered into the record (Paper 41, "Tr.").

B. Real Party in Interest

Samsung Electronics Co., Ltd. identifies itself and Samsung Semiconductor, Inc. as the real parties in interest. Pet. xvi. Netlist, Inc. identifies itself as the real party in interest. Paper 3, 1.

C. Related Matters

The parties indicate this Petition is related to the following district court litigations:

Netlist, Inc. v. Micron Technology, Inc., No. 1:22-cv-00136 (W.D. Tex.);

Netlist, Inc. v. Samsung Electronics Co., Ltd., No. 2:22-cv-00293 (E.D. Tex.);

Netlist, Inc. v. Micron Technology, Inc., No. 2:22-cv-00203 (E.D. Tex.);

Netlist, Inc. v. Samsung Electronics Co., Ltd., No. 2:21-cv-00463 (E.D. Tex.).

Paper 12, 1; Paper 3, 1.

The parties also indicate this Petition is related to the following Board proceedings:

Micron Technology, Inc. v. Netlist, Inc., IPR2023-00205;

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2022-00711;

Micron Technology, Inc. v. Netlist, Inc., IPR2022-00237;

Micron Technology, Inc. v. Netlist, Inc., IPR2022-00236; and

SK hynix Inc. v. Netlist, Inc., IPR2017-00730.

Paper 12, 1–2; Paper 3, 1.

Further, the parties indicate this Petition is related to the following applications:

U.S. Patent Application No. 18/452,554; and

U.S. Patent Application No. 17/114,478.

Paper 12, 2; Paper 3, 2.

D. The '608 Patent

The '608 patent, titled "Memory Module with Timing-Controlled Data Paths in Distributed Data Buffers," relates to a memory system which controls timing of memory signals based on timing information. Ex. 1001, codes (54), (57). Figure 2A, reproduced below, illustrates a memory module. *Id.* at 2:43–45, 4:65–66.

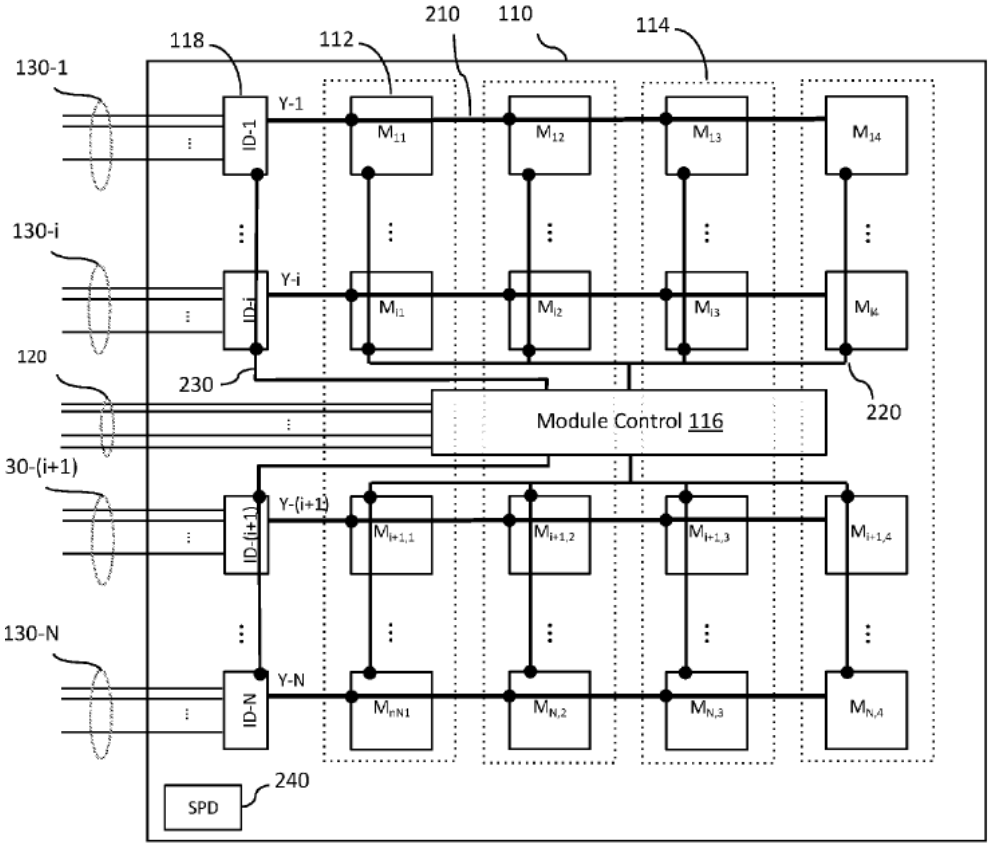


FIG. 2A

As shown in Figure 2A, above, memory module 110 includes module control device 116 and a plurality of memory devices 112. Ex. 1001, 4:65–66, 6:4–5. Memory module 110 further includes control/address signal lines 120 and data/strobe signal lines 130, which are coupled to a memory controller (MCH) (not shown). *Id.* at 4:20–23, 4:65–5:4. Respective groups of data/strobe signal lines 130 are also coupled to respective isolation

devices, or buffers, 118, that is, the group of data/strobe signal lines 130-1 is coupled to isolation device ID-1, for example. *Id.* at 4:23–25; *see id.* at 6:20–25. Furthermore, each isolation device 118 is associated with, and coupled to, a respective group of memory devices via module data/strobe lines 210. *Id.* at 6:17–20, 6:30–32. As an example, along the top of memory module 110 shows isolation device ID-1 "is associated with [a] first group of memory devices M_{11}, M_{12}, M_{13}, and M_{14}, and is coupled between the group of system data/strobe signal lines 130-1 and the first group of memory devices" via module data/strobe lines 210. *Id.* at 6:20–25.

In operation, memory module 110 "perform[s] memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.)." Ex. 1001, 3:29–32. Those commands are transmitted over control/address signal lines 120 and data/strobe signal lines 130 from the memory controller. *Id.* at 3:32–34, 4:66–5:3. For example, "[w]rite data and strobe signals from the controller are received and buffered by the isolation devices 118 before being transmitted to the memory devices 112 by the isolation devices 118." *Id.* at 7:63–66. And "read data and strobe signals from the memory devices are received and buffered by the isolation devices before being transmitted to the MCH via the system data/strobe signal lines 130." *Id.* at 7:66–8:3.

As can be seen in Figure 2A, and as the '608 patent explains, there are "unbalanced" lengths of control wires to respective memory devices which causes a "variation of the timing" of signals due to the variation in wire length. *See* Ex. 1001, 2:20–31; *see also id.* at 8:22–55. To account for timing issues, each isolation device, or data buffer, 118 is "responsible for providing a correct data timing" and "providing the correct control signal timing." *Id.* at 8:56–9:3. In particular, "isolation devices 118 includes signal alignment mechanism to time the transmission of read data signals

based on timing information derived from a prior write operation." *Id.* at 15:23–26. For example, because write signals are received by isolation device 118, isolation device 118 uses that knowledge and determines timing information which is used to "properly time transmission" of a later-read operation. *Id.* at 15:45–50.

E. Challenged Claims

Petitioner challenges claims 1–12 of the '608 patent in the Petition. Pet. 1.

Subsequent to the filing of the Petition, Patent Owner filed a statutory disclaimer under 35 U.S.C. § 253(a) to disclaim claims 6–12 of the '608 patent. Ex. 2001 ("Disclaimer in a Patent Under 37 C.F.R. 1.321(a);" "Electronic Payment Receipt;" "Electronic Acknowledgment Receipt"); *see* 35 U.S.C. § 253(a); 37 C.F.R. § 1.321(a). Because Patent Owner's statutory disclaimer satisfies all regulatory requirements to disclaim claims 6–12, we do not consider Petitioner's challenges to those claims. *See* Ex. 2001; 37 C.F.R. § 1.321(a); *General Electric Co. v. United Techs. Corp.*, IPR2017-00491, Paper 9 (PTAB July 6, 2017) (precedential).

Claim 1 is the only independent claim. Claim 1, which is illustrative, is reproduced below, with bracketed letters provided by Petitioner (*see* Pet. xiii) added to limitations for reference purposes.

> 1. [pre] A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal[1] lines, the memory module comprising:

[1] Data signals lines are referred to as "DQ" signal lines, and data strobe lines are referred to as "DQS" signal lines. *See* Ex. 1001, 10:31–35.

> [a] a module board having edge connections for coupling to respective signal lines in the memory bus;
>
> [b] a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and
>
> [c] memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and
>
> [d] a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, [e] wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal, [f] wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

Ex. 1001, 19:14–55.

F. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–5 of the '608 patent are unpatentable based on the following grounds[2]:

Claim(s) Challenged	35 U.S.C §	Reference(s)/Basis
1–5	103(a)[3]	Hiraishi[4], Butt[5]
1–5	103(a)	Hiraishi, Butt, Tokuhiro[6]
5	103(a)	Hiraishi, Butt, Ellsberry[7]
5	103(a)	Hiraishi, Butt, Tokuhiro, Ellsberry

Pet. 1.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Relying on the testimony of Dr. Wedig, Petitioner proposes that a person of ordinary skill in the art at the time of invention of the '608 patent "would have been someone with an advanced degree in electrical or computer engineering and at least two years of work experience in the field of memory module design and operation, or a bachelor's degree in such

[2] Because Patent Owner has disclaimed claims 6–12 of the '608 patent, we do not further address these claims, or associated grounds, because they are no longer at issue in this proceeding.
[3] The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. § 103, and was effective on March 16, 2013. Because the '608 patent claims priority before the effective date of the applicable AIA amendments (*see* Ex. 1001, code (60)), we refer to the pre-AIA version of 35 U.S.C. § 103.
[4] US 2010/0312956 A1, published December 9, 2010 (Ex. 1005, "Hiraishi").
[5] US 2007/0008791 A1, published January 11, 2007 (Ex. 1029, "Butt").
[6] US 8,020,022 B2, issued September 13, 2011 (Ex. 1006, "Tokuhiro").
[7] US 2006/0277355 A1, published December 7, 2006 (Ex. 1007, "Ellsberry").

engineering disciplines and at least three years of work experience in the field." Pet. 2 (citing Ex. 1003 ¶ 37). Petitioner further proposes that a skilled artisan "would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of computer memories, including DRAM and SDRAM devices that were compliant with various standards, and how they interact with other components of a computer system, such as memory controllers," and "would also have been familiar with the structure and operation of circuitry used to access and control computer memories and other components of a memory system, including sophisticated circuits such as ASICs and CPLDs, as well as low level circuits such as data buffers, tri-state buffers, flip flops and registers." *Id.* at 2–3 (citing Ex. 1003 ¶ 37).

Patent Owner asserts that, for the purposes of the Patent Owner Response, it applies the level of ordinary skill in the art proposed by Petitioner. PO Resp. 12.

In determining the level of ordinary skill in the art, various factors may be considered, including the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (citation omitted). The level of ordinary skill in the art is also reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). For purposes of this Decision and with the exception of the qualifier "at least" with respect to experience which renders the level of ordinary skill in the art ambiguous and may encompass levels beyond ordinary, we adopt the assessment offered by Petitioner as it is consistent with the '608 patent and the asserted prior art.

B. Claim Interpretation

In this *inter partes* review, claims are construed using the same claim construction standard that would be used to construe the claims in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b) (2021). Under the principles set forth by our reviewing court, the "words of a claim 'are generally given their ordinary and customary meaning,'" as would be understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

In the Petition, Petitioner asserted that "the Board need not expressly construe any claim term because the prior art invalidates the claims under any plausible construction, in accordance with 37 C.F.R. §42.100(b)," but offered references to portions of the '608 patent as examples of usage of certain claim terms. Pet. 7–8. Petitioner did not present any proposed construction for the term "data path." *See id.*

In the Preliminary Response, Patent Owner presented a footnote stating:

> Element 1(f) recites 'the data path corresponding to the each data [DQ] signal line . . . " and "a delay circuit configured to delay a signal through the data path . . .' Pet., xiii. Hence, the signal that is claimed to be delayed is the DQ signal, not the DQS signal.

> Petitioner's analysis conflates DQ and DQS and does not show DQ, instead of DQS, is being delayed.

Prelim. Resp. 10, n.2.

In the Patent Owner Response, Patent Owner argues that some of Petitioner's assertions of invalidity fail because Petitioner improperly included strobe signal lines in the data path so the prior art teachings fail. *See* PO Resp. 18–24. For instance, Patent Owner argues that, in Petitioner's assertions, Hiraishi's DQS strobe signal line is included in the "data path" mapped to its Figure 5, "[b]ut the claims clearly exclude strobe signals lines from the recited 'data path.'" *Id.* at 19–20. Patent Owner also refers to Hiraishi's Figure 3, which distinguishes between data signal lines carrying data signals and strobe paths carrying strobe signals. *Id.* at 20–21. Patent Owner points to Hiraishi's Figures 15 and 16, asserting that these show the distinction of strobe paths and data paths. *Id.* at 21–23. Patent Owner argues that the Specification and claim language of the '608 patent also support "that strobe signal lines form a strobe path and data signal lines form a data path." *Id.* at 23–24 (citing Ex. 2013 ¶¶ 70–78).

In Reply, Petitioner argues that Patent Owner's attempt to exclude "strobe signal lines" from "*data path*[*s*]" is precluded by the Final Written Decision rendered in IPR2022-00236 ("the -00236 IPR"). Pet. Reply 1. Petitioner asserts that the -00236 IPR involved U.S. Patent No. 9,824,035 ("the '035 patent"), which is the parent of the '608 patent. *Id.* Petitioner points to the -00236 IPR, where Osanai was the asserted prior art, and contends that Patent Owner admits that Osanai is the same as Hiraishi in all material aspects. *Id.* (citing Prelim. Resp. 5). Petitioner also refers to the Board's statement that "each buffer circuit . . . includes data paths for transmitting data and strobe signals" and "[t]hese data paths connect lines L0

to lines L1 and L2." *Id.* at 2 (quoting Ex. 1066, 35; referring to *id.* at 25–26) (emphasis omitted). Petitioner argues that the Board's decision in -00236 IPR precludes Patent Owner's arguments. *Id.* at 4 (citing *Google LLC v. Hammond Dev. Int'l, Inc.*, 54 F.4th 1377, 1381 (Fed. Cir. 2022); *Mobile Tech, Inc. v. InVue Security Prods. Inc.*, IPR2018-00481, Paper 29, 11–17, 18–19, 33 (PTAB July 16, 2019); *B & B Hardware, Inc. v. Hargis Indus.*, Inc., 575 U.S. 138, 148 (2015); Restatement (Second) of Judgments §§ 13, 27; *SSIH Equip. S.A. v. ITC*, 718 F.2d 365, 370 (Fed. Cir. 1983)).

Petitioner additionally contends that Patent Owner tries to conflate the "*data path*" with the "*data signal line*." Pet. Reply 4. Petitioner asserts that in the '608 patent the claimed data path through the buffer circuit is not the claimed data signal line. *Id.* at 4–5 (citing Pet. 3–4; Ex. 1001, 3:57–60, 4:23–25, Figs. 1, 2C). Petitioner argues that "[w]hile the claimed 'data path' through each 'buffer circuit' illustrated above [Figs. 1, 2C] 'correspond[s] to each data signal line' as required by [1.e], that does not mean the 'data path' is a 'data signal line,'" as Patent Owner suggests. *Id.* at 5 (citing PO Resp. 20–23) (emphasis omitted). Petitioner contends that a "data path" is "a broader concept," that is "the course or direction in which a . . . thing is moving." *Id.* at 5 (citing Ex. 1087). Petitioner asserts that, "consistent with that broad concept," the Specification discloses that "each buffer circuit [] . . . is in the data paths between the respective group of memory devices [] and the memory controller." *Id.* (quoting Ex. 1001, 3:57–:60 (emphasis omitted), citing 6:59–62, 15:17–19; Ex. 2012, 47:20–48:2). Petitioner further argues the Specification teaches that the entire buffer circuit is in the "data path" and that dependent claim 10 refutes Patent Owner's "argument that the 'data path' cannot include 'data strobe signal lines': 'wherein the each respective buffer circuit includes a first data path for transmitting a

strobe signal." *Id.* at 5–6 (citing Pet. xv, 67–71; Ex. 2012, 45:7–46:2, 49:22–50:13, 144:22–145:10) (emphasis omitted). Petitioner contends that Patent Owner admits that both DQ data signals and DQS strobe signals go through the buffer in Figure 3. *Id.* at 6 (citing PO Resp. 21; Ex. 1001, 2:46–47, 8:4–8, 10:31–61). Petitioner also argues that limitation 1[j] of the related '035 patent refutes Patent Owner's argument, and Patent Owner's expert admitted that a related patent (U.S. Patent No. 10,860,506 ("the '506 patent"), a continuation of the '608 patent) disclosed "a strobe signal through the data path." *Id.* (citing Ex. 1031, 19:44; Ex. 1076 ¶ 34; Ex. 1074, 20:24–22:11). Petitioner further asserts that Patent Owner's arguments that Figures 15 and 16 support its construction are incorrect. *Id.* at 6–8 (citing PO Resp. 22–23; Ex. 1001, Figs. 15, 16). Petitioner contends that in these figures, the data signals and strobe signals in respective transmission lines are eight subparts of the broader "data path," "which includes both data and strobe signals that travel together." *Id.* at 8 (emphasis omitted). Petitioner also argues, with respect to Figure 16, that the Federal Circuit has warned against confining the claims to specific embodiments. *Id.* at 9 (citing *Weber, Inc. v. Provisur Techs., Inc.*, 492 F.4th 1059, 1070 (Fed. Cir. 2024)).

Petitioner also asserts that Patent Owner's attempt to divorce a strobe signal from the data path is contrary to the testimony of the experts, and it was known "that the strobe signal (DQS) is essential to the transmission of the data signal (DQ), which is why both signals must travel together within a 'very tight tolerance.'" Pet. Reply 9 (emphasis omitted). Petitioner contends that Patent Owner admits that "DQS signals . . . ensur[e] accurate timing for sampling/capturing DQ data," and Patent Owner has argued that DQ/DQS signals must remained aligned with each other. *Id.* at 10 (citing PO Resp. 6; Ex. 1086, 22–23 (demonstrative from IPR2022-00711))

(emphasis omitted). Petitioner contends that both Butt and Hiraishi disclose data paths that include a DQS strobe signal and a corresponding DQ data signal. *Id.* at 10–12.

Patent Owner responds with the assertion that "the claims of the '608 patent recite 'a data path corresponding to each data signal line,' but not the strobe signal line, in the 'respective set[s] of data/strobe signal lines.'" PO Sur-reply 1 (citing Ex. 1001, 19:29–45, 4:20–32, 6:11, 6:19–20, 8:2–3, 10:31–35, Fig. 3) (emphasis omitted). In support, Patent Owner refers to annotated Figure 3 of the '608 patent reproduced below. *Id.* at 1–2.

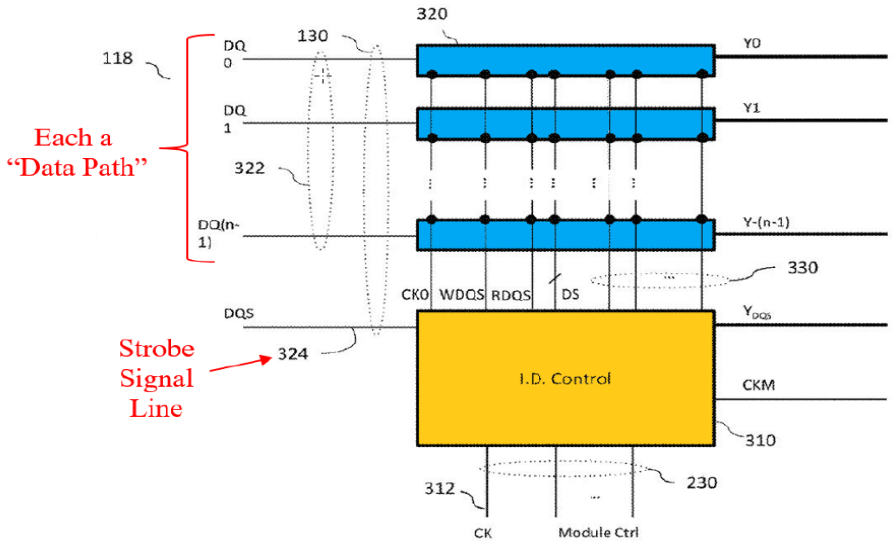


FIG. 3

Annotated Figure 3, above, depicts isolation device 118 and inputs and outputs to/from DQ routing circuits 320 and to/from I.D. Control 310. *See* Ex. 1001, 10:31–11:8. Dr. Mangione-Smith testifies that isolation device 118 is referred interchangeably with a buffer circuit. Ex. 2013 ¶ 70 (citing Ex. 1001, 3:27–29, 4:30). In association with Figure 3 of the '608 patent, Patent Owner refers to the description in the '608 patent Specification that states:

> . . . as shown in FIG. 3, each group of signal lines 130 include a set of n data (DQ) signal lines 322 each for transmitting one of a set of data signals DQ_0, DQ_1, . . . , DQ_{n-1}, and at least one strobe (DQS) signal line 324 for transmitting at least one strobe signal DQS.

Ex. 1001, 10:31–35 (cited in PO Sur-reply 1). Patent Owner contends that the strobe signal line is not part of the claimed "data path" that corresponds to each "data signal line" because "there is only a single DQS line for each n-bit group of data signal lines." PO Sur-reply 2 (citing Ex. 1001, Figs. 3, 4A–4B, 11:20–45). Dr. Mangione-Smith identifies other figures and descriptions in the '608 patent that identify that there are different data paths identified on differing data lines and strobe lines, respectively. *See* Ex. 2013 ¶¶ 73–76.

Patent Owner also asserts that the '035 patent confirms that the '608 patent's claimed "data path" excludes strobe signal lines. PO Sur-reply 1. Patent Owner argues that claim 1 of the '035 patent uses the term "respective" in "data paths for transmitting *respective* data and strobe signals," which indicates that there can be data paths for strobe signals and separate data paths for data signals. *Id.* (citing Ex. 1031, 19:35–37). Patent Owner further argues that claims 15 and 16 of '608 patent recite separately "first" and "second" "data path[s]" for strobe signals and data signals, respectively, which provides further support for separate data paths for data signals and strobe signals, respectively. *Id.* (citing Ex. 1031, 20:60–21:2).

Patent Owner further responds that there is no estoppel that applies as a result of the decision in the -00236 IPR because the instant proceeding involves different issues of patentability that are not essential to the -00236 IPR. PO Sur-reply 4 (citing *Google* LLC, 54 F.4th 1377, 1381 (Fed. Cir. 2022)). Patent Owner argues that the '608 patent and the '035 patent in

the -00236 IPR recite different "data paths." *Id.* at 5. Patent Owner further asserts that there was unrebutted expert testimony that there were "important differences" between the '608 patent claims and '035 patent claims. *Id.* at 5 (citing Ex. 2013 ¶ 197). Patent Owner refers to claim language of the '608 patent concerning signaling for the delay circuit and the module control signal and system command signals, where the '035 patent does not have comparable language. *Id.* (citing Ex. 1001, 19:52–55, 19:21–26, 19:15–18, 19:29–32). Patent Owner contends that this difference is significant because, with these requirements, not all the signals sent by Hiraishi's command/address/control register buffer 400 (alleged to be the "module control device") to the data register buffer 300 (alleged to be "buffer circuits") would qualify as a claimed "module control signal." *Id.* at 5–6. Patent Owner additionally refers to the different unpatentability theories in this case and the -00236 IPR. *Id.* at 6. For instance, Patent Owner contends, in the -00236 IPR the Board relied upon "Hiraishi's input ("INB") buffers to find that there was sufficient teaching for 'controlling the timing of the data and strobe signals on the data paths on which those signals travel,'" whereas in this proceeding Petitioner's expert testified that the INB is not part of the "delay circuit." *Id.* (citing Ex. 2023, 36; Ex. 2013 ¶ 199; Ex. 2012, 31:23–25).

What we consider here is interpretation of the language of limitation 1[e], together with limitation 1[f], and note that we are not performing claim construction of a specific claim term or phrase *per se*. Claim 1 of the '608 patent recites that "each respective buffer circuit including *a data path corresponding to each data signal line in the respective set of data/strobe signal lines*" [limitation 1[e]] and "wherein the *data path corresponding to the each data signal line* includes" . . . "a delay circuit configured *to delay a*

signal through the data path by an amount . . . " [limitation 1[f]]. Ex. 1001, 19:36–55 (emphasis added). The operative issue is the identification of the "data path" that is claimed in claim 1. The claim differentiates between data signal lines and strobe signal lines. Limitation 1[e] identifies that "a data path" corresponds to the data signal line in the set of data/strobe signal lines; that is, it is a data path that is in the data signal line. The data path claimed, therefore, is not in a strobe signal line of the set of data/strobe signal lines. Limitation 1[f] confirms this understanding, reciting "the data path," (with the antecedent of "a data path" of limitation 1[e]), that corresponds to each data signal line, and which includes a delay circuit that delays a signal through the data path. Patent Owner refers to Figures 3, 4A, and 4B of the '608 patent, which confirms this understanding of the language of claim 1 in that it provides written description support for the reading of the explicit language of claim 1. *See* PO Sur-reply 1–2. These figures, as well as their associated descriptions, support that there are different transmission lines (data paths) with a separate signal transmission line for transmitting/receiving data signals and a separate strobe line for transmitting/transmitting strobe signals. See Ex. 1001, 10:31–11:8, 11:20–45, Figs. 3, 4A–4B, *see also id*. code (57) (identifying that the "data path" corresponds with the data signal line in the set of data/strobe signal lines).

We do not agree with Petitioner's argument that Patent Owner conflates "data path" with the "data signal line." A reasonable plain meaning of "data path" is that it is the path that data is transmitted on[8], and,

[8] The parties do not offer a proposed construction for the term "data path" itself; rather the issue raised, as discussed above, is which signal lines are in the claimed data path. *See generally* Pet.; PO Resp.; Pet. Reply; PO Sur-reply.

as discussed above, the claimed "data signal line" is the actual data signal line of the respective set of data/strobe lines. We also do not agree with Petitioner's arguments that the data path though the buffer circuit is not the claimed data signal and that that the entire buffer circuit is in the claimed "data path" based on some figures of the '608 patent. *See* Pet. Reply 4–6. As discussed above, there is support in the Specification for the interpretation of the language of claim 1 that the data path as recited in claim 1 is in the data signal lines, that are separate from the strobe line, as shown in Figure 3, wherein isolation device 118 is a buffer. *See* Ex. 1001, 3:27–29, 10:31–11:8. Although the buffer may receive both data and strobe signals, as shown in Figure 3, the data signal lines, which are on the claimed data path, carry data signals only.

We also do not agree with Petitioner's assertion that dependent claim 10 refutes that the "data path" cannot include "data strobe signal lines." Pet. Reply 6. Claim 10 recites that "respective buffer circuit includes a first data path for transmitting a strobe signal" and "a second data path for transmitting a first data signal." Ex. 1001, 20:48–53. We agree with Patent Owner (PO Sur-reply 3) that claim 10 recites new elements, namely a "first data path" and "second data path," which are different than the element of "a data path" of claim 1. *See Phillips*, 415 F.3d at 1315 ("[T]he presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim."); *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 910 (Fed. Cir. 2004) ("[W]here the limitation that is sought to be 'read into' an independent claim already appears in a dependent claim, the doctrine of claim differentiation is

at its strongest."). Moreover, claim 10 reinforces that there are separate data paths for data signals and for strobe signals.

Although Petitioner asserts that data signals and strobe signals in respective transmission lines in Figures 15 and 16 of the '608 patent are "eight subparts" of the "data path," (Pet. Reply 8–9), we do not agree; rather these figures also serve to support that there are separate data paths for data signals and for strobe signals. Additionally, although Petitioner suggests that the references to portions of the '608 patent serve to confine the claims to specific embodiments (Pet. Reply 9), we do not agree. As discussed above, the evaluation of "data path" in claim 1 is based on a reading of the language of the claim and any references to the patent's disclosures serves to confirm that there is written description support of this plain reading. Further, although Petitioner asserts that it was known that the strobe signal is essential to the transmission of the data signal and that both data and strobe signals "must travel together within a 'very tight tolerance,'" (Pet. Reply 9), multiple disclosures of the '608 patent, as discussed above, show that the data signal and strobe may travel on different transmission lines.

Petitioner also contends that there is there is a preclusive effect of the Board's finding for the term "data path" for claims of the '035 patent in the -00236 IPR. *See* Pet. Reply 1–4; Ex. 1066, 5–7, 22–43, 46–52. Petitioner relies on the Board's statement in the -00236 IPR relating to claims of the '035 patent that "each buffer circuit . . . includes data paths for transmitting data and strobe signals" and "[t]hese data paths connect lines L0 to lines L1 and L2" in Osanai.[9] *See* Pet. Reply 2 (emphasis omitted)

[9] Petitioner refers to Patent Owner's statement that Osanai is "the same as Hiraishi in all material respects," and asserts that the Petition relies on the same data paths connecting L0 to L1/L2 here. Pet. Reply 1–2.

(quoting Ex. 1066, 35). We do not find that the Board's statement in the -00236 IPR acts to preclude the interpretation here of the term "data path" of claim 1 of the '608 patent, as discussed above.

As discussed in *Google LLC*, the party seeking to invoked collateral preclusion must demonstrate that:

> (1) *the issue is identical to one decided in the first action;* (2) the issue was actually litigated in the first action; (3) resolution of the issue was essential to a final judgment in the first action; and (4) [the party against whom collateral estoppel is being asserted] had a full and fair opportunity to litigate the issue in the first action.

Google LLC, 54 F.4th at 1381 (citing *In re Freeman*, 30 F.3d 1459, 1465 (Fed. Cir. 1994) (emphasis added)). The issues in this proceeding and those at issue in the -00236 IPR are not identical. The claims of the '035 patent and the instant '608 patent are different. Claim 1 of the '035 patent recites "each respective buffer circuit including *data paths for transmitting respective data and strobe signals* associated with the first memory operation and logic configured to respond to the module control signals by enabling the data paths," "wherein the logic is further configured to obtain timing information based on one or more signals . . . to control timing of the respective data and strobe signals on the data paths." Ex. 1031, 19:35–45. Claim 1 of the '035 patent explicitly recites that the data paths have data and strobe signals transmitted on them. That is unlike claim 1 of the '608 patent at issue here—claim 1 of the '035 patent does not recite that the "data

path" is "corresponding to *each data signal line* in the respective set of data/strobe signal lines," as claim 1 of the '608 patent does.

To support the alleged preclusive effects of the -00236 IPR, Petitioner refers to *B & B Hardware*, which quotes the Restatement, which states that "subject to certain well-known exceptions,"

> When an issue of fact or law is actually litigated and determined by a valid and final judgment, and the determination is essential to the judgment, the determination is conclusive in a subsequent action between the parties, whether on the same or a different claim.

Restatement (Second) of Judgments § 27, p. 250 (1980) (quoted by *B & B Hardware*, 575 U.S. at 148). The *Google LLC* Federal Circuit case, referenced by Petitioner, further states that:

> [C]ollateral estoppel requires that the issues of patentability be identical. *Ohio Willow Wood*, 735 F.3d at 1342. Thus, collateral estoppel may apply even if the patent claims 'use slightly different language to describe substantially the same invention,' so long as '*the differences between the unadjudicated patent claims and adjudicated patent claims do not materially alter the question of invalidity*.' *Id*. Whether the differences between the patent claims materially alter the question of patentability is a legal conclusion based on underlying facts.

Google LLC, 54 F.4th at 1381 (emphasis added).

As discussed above, and as Patent Owner argues, claim 1 of the '608 patent and claim 1 of the '035 patent in the -00236 IPR recite different "data paths." PO Sur-reply 5. Patent Owner also asserts, and we agree, that there is unrebutted expert testimony from Dr. Mangione-Smith that there were other "important differences" between the '608 patent and '035 patent claims. *Id*. at 5 (citing Ex. 2013 ¶ 197). Dr. Mangione-Smith's unrebutted testimony is that "[t]he '035 patent then uses the 'timing information' to 'control timing of respective data and strobe signals,' while the '608 patent

delays a signal through a data path corresponding to a data signal line with a delay circuit that is included in the data path," as well as that the '608 patent recites both a tristate buffer and delay circuit in the data path, which the '035 patent does not. Ex. 2013 ¶ 197. Petitioner additionally refers to Dr. Mangione-Smith's testimony in an expert report relating to a proceeding involving the '506 patent for arguments on "data path." Pet. Reply 6. However, claim 1 of the '506 patent is also different than that of the '608 patent, so we do not find that language relevant as to how we should interpret the language of claim 1 of the '608 patent.

Patent Owner also asserts that the '608 patent claims require a delay circuit on the data path be configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals, where the module control signals are in response to system command signals received from the control/address signal lines in the memory bus. PO Sur-reply 5 (citing Ex. 1001, 19:52–55, 19:21–26, 19:15–18). We agree, and discern no similar recitals in the '035 patent. *See* Ex. 1031. Additionally, the'608 patent recites the use of system command signals to result in module command signals used by memory devices for performing memory operations, which are not recited in the '035 patent claims. *See* Ex. 1001, 19:24–26, 19:29–32; Ex. 1031. Patent Owner also contends, and we agree, that the differences in the '608 patent here and the '035 patent in the -00236 IPR are significant because, with the claim 1 requirements of the '035 patent, not all the signals sent by Hiraishi's command/address/control register buffer 400 (alleged to be the module control device) to the data register buffer 300 (alleged to be buffer circuits) would qualify as a claimed "module control signal." *See* PO

Sur-reply 5–6 (citing Ex. 1001, 19:21–26, 19:15–18; Ex. 1005, Ex. 1005 ¶¶ 147, 148, Figs. 11, 12, 15).

We also agree with Patent Owner that the unpatentability theories in this *inter partes* review and that of the -00236 IPR are different. In the -00236 IPR, there was no ground asserted based on moving Tokuhiro's delay element out of the memory controller and into the data buffer which is at issue here. Further, in the -00236 IPR, the Board relied upon Osanai's input buffers for the finding that there was a teaching of "controlling the timing of the data and strobe signals on the data paths on which those signals travel," while here Dr. Wedig testifies that the input buffers were not part of the delay circuit. *See* Ex. 2023, 36; Ex. 2013 ¶ 199; Ex. 2012, 31:23–25 ("Q. . . INB buffers [of Hiraishi], are those part of the delay circuit as well? A. No, they're not.").

Thus, in light of the differences between the claims of the '608 patent and the '035 patent and the differences in the invalidity issues in the instant proceeding and the -00236 IPR, we find that no estoppel applies based on the Board's findings in the -00236 IPR.

At oral hearing. Petitioner first argued that during the prosecution of the '608 patent, the Patent Office stated that the claims of the '608 patent and the '035 patent were not patentably distinct. *See* Tr. 17:23–18:15; Ex. 1002, 102. Even if we were to consider this late-raised issue, the Patent

Office was addressing an obvious-type double patenting issue and not addressing the claim language. *See* Ex. 1002, 102.

Accordingly, claim 1 recites that a "data path" which corresponds to data signal lines carrying data signals and not to strobe signal lines carrying strobe signals.

C. Principles of Law

A patent claim is unpatentable as obvious "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." 35 U.S.C. § 103(a); *see also KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective indicia of nonobviousness.[10] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

D. Asserted Obviousness of Claims 1–5 Over Hiraishi and Butt

Petitioner contends that claims 1–5 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Hiraishi and Butt. Pet. 15–59. In support, Petitioner also relies upon the Wedig Declaration. Ex. 1003.

In the Patent Owner Response, Patent Owner focuses on limitations 1[e] and 1[f] and asserts that neither Hiraishi or Butt teaches these

[10] No evidence of objective indicia of nonobviousness is in the evidence of record. *See generally* Pet.; PO Resp.; Pet. Reply; PO Sur-reply.

limitations. PO Resp. 1–4, 18–57. In support, Patent Owner relies on the Mangione-Smith Declaration. Ex. 2013.

In Reply, Petitioner disputes Patent Owner's interpretation of "data path" in claim 1, as discussed above, and contends that Hiraishi teaches the limitations under the interpretation that Petitioner advocates. Pet. Reply 1–12. Petitioner also asserts that even under Patent Owner's interpretation, the combination of Hiraishi and Butt teaches the limitations. *Id.* at 12–31.

In Sur-reply, Patent Owner contends that Petitioner's Reply substantially revised its unpatentability theory. PO Sur-reply 7–9. Patent Owner argues, however, that even under Petitioner's "re-written" theory, Hiraishi and Butt still fail to teach the claim limitations. *Id.* at 9–18.

We begin our discussion with brief summaries of Hiraishi and Butt, and then address the evidence and arguments presented. We then first evaluate Petitioner's evidence and argument under its original assertions in the Petition, and then address the revised assertions that Petitioner presents in Reply, including an assessment of whether the new assertions are permissible in a reply.

1. Hiraishi (Ex. 1005)

Hiraishi relates to a memory module having memory chips and data register buffers arranged in a manner which allows for a high data transfer rate. Ex. 1005, code (57). Figure 1, reproduced below, "is a schematic diagram of a configuration of a memory module." *Id.* ¶ 13.

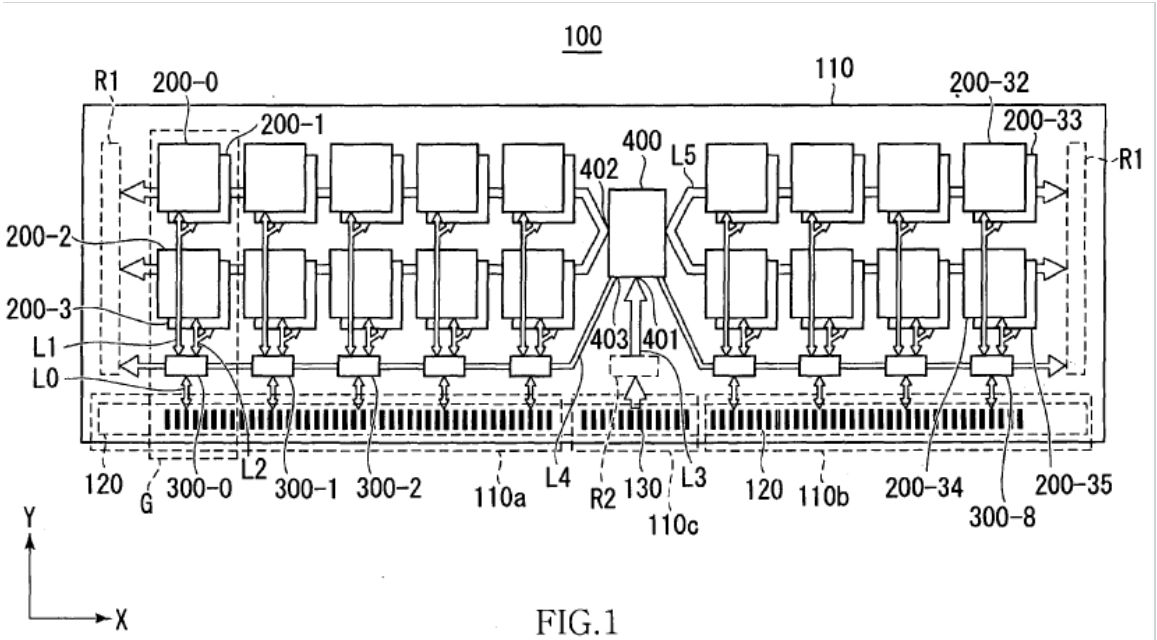


FIG.1

As shown in Figure 1, memory module 100 includes a plurality of memory chips 200 mounted on module substrate 110. Ex. 1005 ¶ 45. Further, memory module 100 includes nine data register buffers 300-0 to 300-8 and command/address/control register buffer 400. *Id.* ¶ 46. Still further, memory module 100 includes "data connectors 120 [which] are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and [a] memory controller" electrically connected to the connectors. *Id.* ¶¶ 47–48 (memory controller not shown).

As can be seen in Figure 1, and as further detailed in Figure 7, "data register buffer 300 intervenes between the data connector[] 120 and the memory chips 200." Ex. 1005 ¶ 103. Figure 7, reproduced below, is a connection diagram of memory module 100. *Id.* ¶ 19.

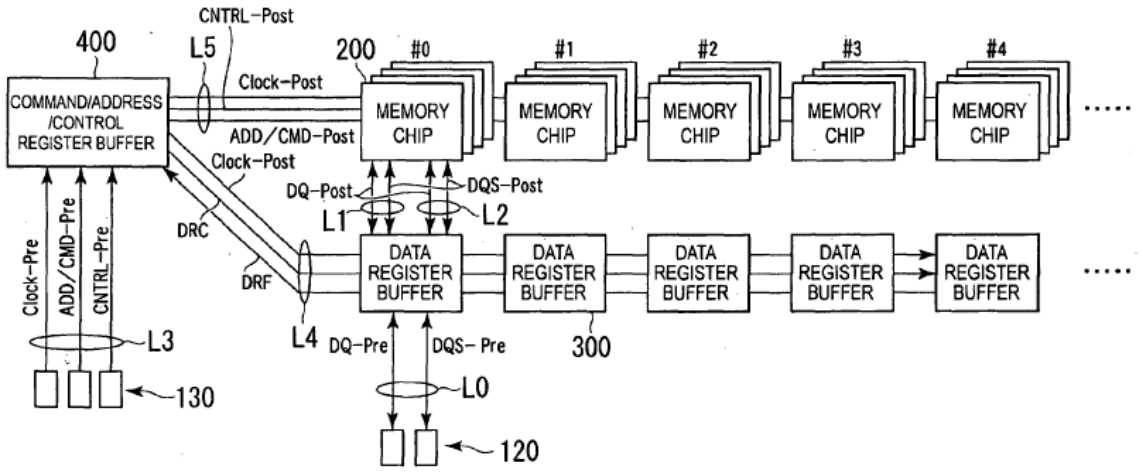


FIG.7

As shown in Figure 7, above, "data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2." Ex. 1005 ¶ 103. "[A] plurality of data transferred through the data line L0 is represented by data DQ-Pre, and a plurality of data transferred through the data lines L1 and L2 is represented by data DQ-Post."[11] *Id.* In addition, "a data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post." *Id.*

Further, "[a]lthough the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post."

[11] Similar to the '608 patent, in Hiraishi, "DQ" refers to a data signal and "DQS" refers to a data strobe signal (*see* Ex. 1005 ¶ 91), and in Hiraishi, "DQ-Pre" refers to data signals input to Data Buffer Register Buffer and "DQ-Post" refers to data signal output from Data Buffer Register (*id.* ¶ 107, Fig. 7).

Ex. 1005 ¶ 104. As such, "it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the memory controller." *Id.* Hiraishi "adjust[s] a write timing or a read timing in consideration of a propagation time of a signal" via leveling operations. *Id.* ¶ 140. The write leveling and read leveling operations are provided via write leveling and read leveling circuits in the data register buffer, as shown in Figure 5, which is a block diagram of the configuration of the data register buffer 300 and is reproduced below. *Id.* ¶ 83.

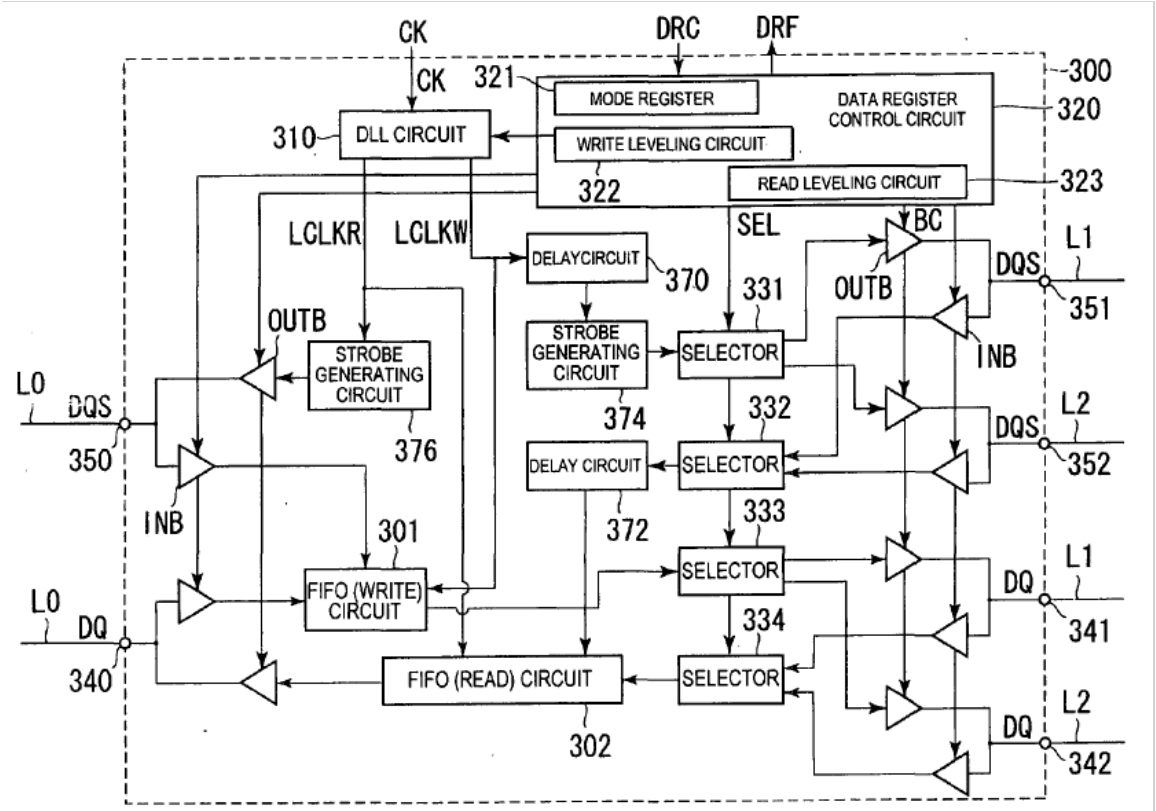


FIG.5

As shown in Figure 5, above, data register buffer 300 includes a data register control circuit 320 having write leveling circuit 322 and read leveling circuit 323. Ex. 1005 ¶ 90. The write leveling and read leveling operations "adjust a write timing or a read timing in consideration of a propagation time of a

signal." *Id.* ¶ 140. For example, in a write operation, "[b]ecause it takes a certain amount of propagation time until the data strobe signal DQS reaches the memory chip 200, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip 200 side." *Id.* ¶ 143. To compensate for that, "write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS." *Id.* ¶ 145. The read leveling operation is used to adjust signal timing for the read operation. *See id.* at ¶¶ 147–151.

2. Butt (Ex. 1029)

Butt relates to DQS strobe centering in memory systems such as DDR [double data rate] memories. Ex. 1029 ¶¶ 2–3. Specifically, Butt describes calibrating a data valid window by setting a base delay for one or more datapaths to a predetermined value, determining an optimum offset delay value for each data path based on actual memory access, and delaying a read data strobe signal based on both the base delay and optimum offset delay for each datapath. *Id.* ¶ 5. Butt's Figure 2, reproduced below, shows a detailed block diagram of a circuit that may serve as a memory interface between a memory controller and a memory. *See id.* ¶¶ 15–17.

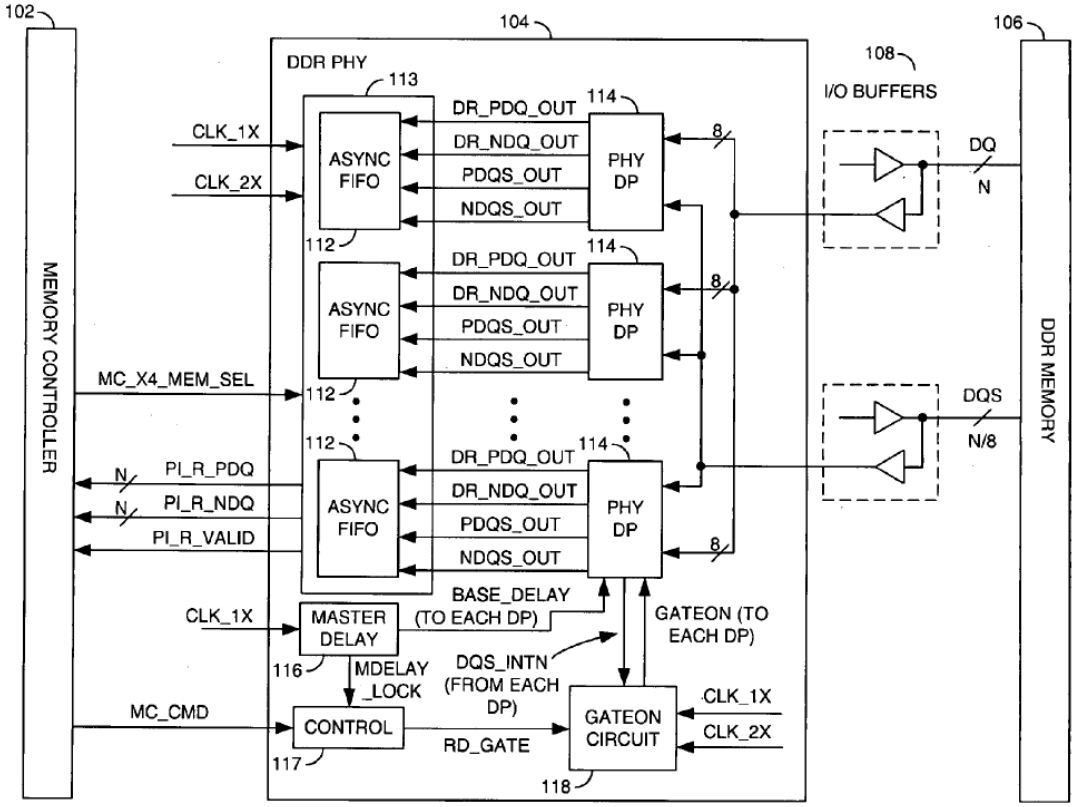


FIG. 2

As shown in Figure 2, above, circuit 104 comprises a number of physical read datapaths 114 that "may be configured to receive (i) a respective portion of the read data signals DQ from the DDR memory 106, (ii) a respective read data strobe signal of signals DQS associated with the respective portion of the received read data signals and (iii) a gating signal . . . from the programmable gating signal generator 118." Ex. 1029 ¶ 17. "[A]synchronous FIFOs 112 may be configured to interface the physical read datapaths 114 with the memory controller 102." *Id.* In operation, "the read datapaths 114 are generally programmable from when the data/strobe pairs DQ/DQS are received at the input to the circuit 104, to sampling the

read data with the read data strobe signal DQS, and passing the data to the memory controller 102." *Id.* ¶ 20.

3. Discussion of the Petition's Original Contentions and Associated Patent Owner Responses

We focus on limitation 1[f]. Petitioner contends that the combination of Hiraishi and Butt discloses that each buffer circuit includes a data path corresponding to each data signal line in the respective set of data/strobe signal lines. Pet. 33. In particular, Petitioner relies on the annotated versions of Hiraishi's Figure 5, reproduced below, with orange highlighting, (solid highlighting representing data signals and broken highlighting representing strobe signals), depicting alleged data paths for respective read and write operations. *Id.* at 33–34.

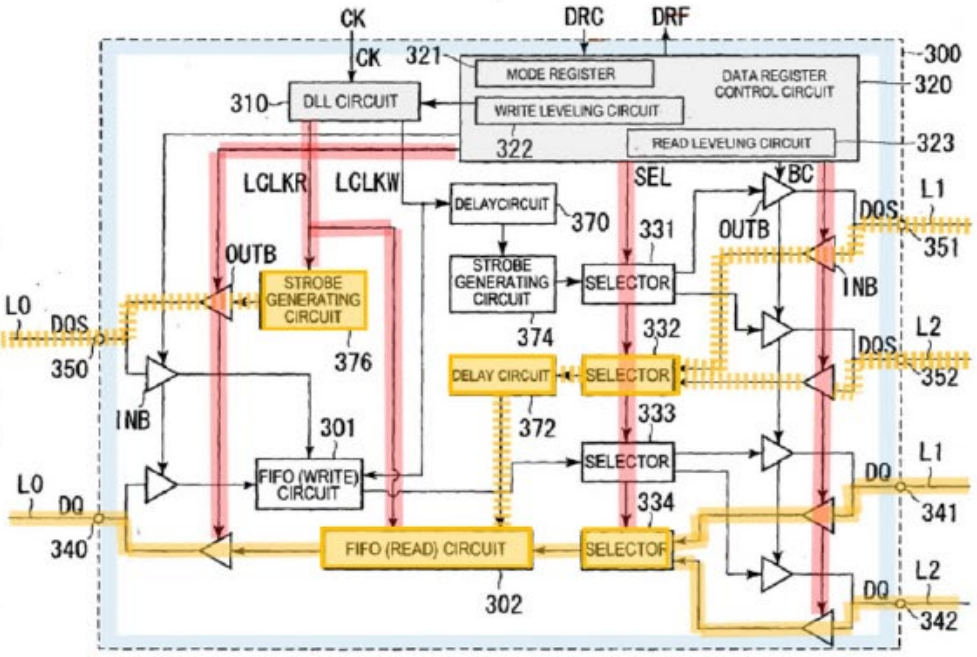


FIG.5

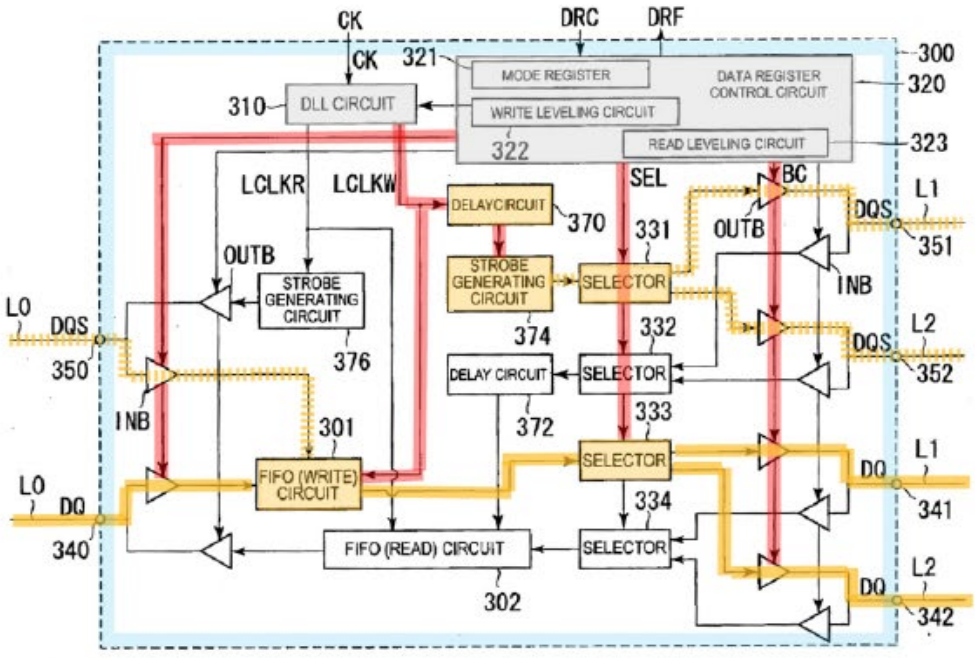


FIG.5

Pet. 34. Petitioner's annotated versions of Figure 5 of Hiraishi, above, depict the elements of a data register buffer showing Petitioner's alleged

data path for read and write operations, respectively. *Id.* Specifically, Petitioner argues that "during memory read or write operations, each respective buffer circuit buffers the data in respective FIFO Read or Write circuits between the data/strobe terminals 340/350 on the left of Figure 5 and the data/strobe terminals 341/342 and 351/352 on the right in Figure 5." *Id.* at 35 (citing Ex. 1003 ¶ 143; Ex. 1005 ¶ 84). Dr. Wedig provides supporting testimony (Ex. 1003 ¶ 142), and refers to Hiraishi's disclosure that:

> As shown in FIG. 5, the data register buffer 300 includes a FIFO (Write) circuit 301 and a FIFO (Read) circuit 302. The FIFO (Write) circuit 301 buffers data DQ that is supplied via an input/output terminal 340 with a data strobe signal DQS that is supplied via an input/output terminal 350. The FIFO (Read) circuit 302 buffers data DQ that is supplied via an input/output terminal 341 or 342 with a data strobe signal DQS that is supplied via an input/output terminal 351 or 352. A strobe generating circuit 376 generates a data strobe signal DQS to be supplied to the data connectors 120, in synchronization with an internal clock LCLKR that is generated by a DLL circuit 310. A strobe generating circuit 374 generates a data strobe signal DQS to be supplied to the memory chip 200, in synchronization with an internal clock LCLKW that is generated by the DLL circuit 310.

Ex. 1005 ¶ 84 (quoted in Ex. 1003 ¶ 142 (emphasis omitted)).

Petitioner also identifies alleged data paths in Butt, arguing that, "[s]imilarly, Butt discloses that a circuit between a memory controller and DDR memory devices uses strobe signals to sample the data signals and buffers the data samples in FIFOs," and that "such a circuit is an implementation of a 'data path.'" Pet. 35–36 (citing Ex. 1003 ¶ 144; Ex. 1029 ¶ 17, Figs. 2, 3A). Petitioner refers to annotated versions of Figures 2 and 3A of Butt, reproduced below.

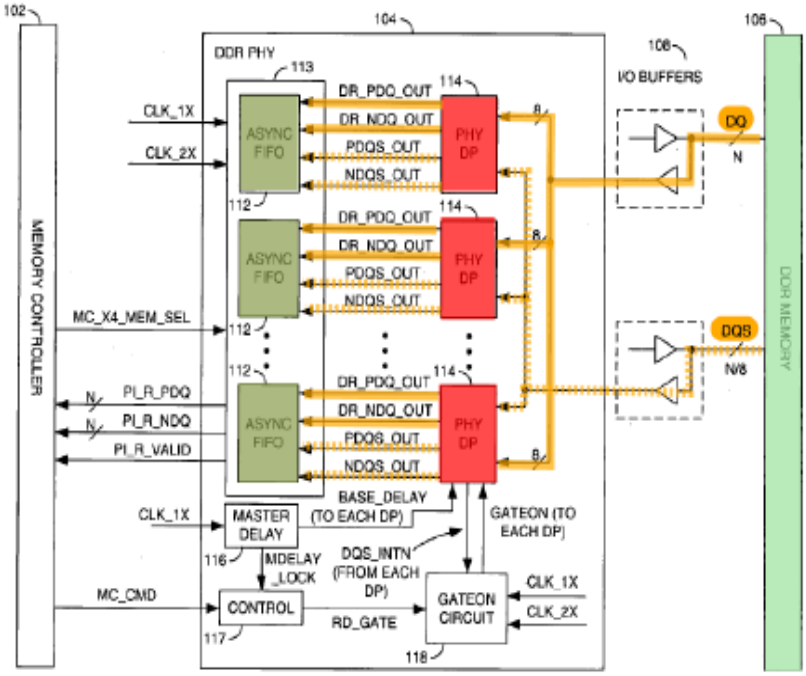


FIG. 2

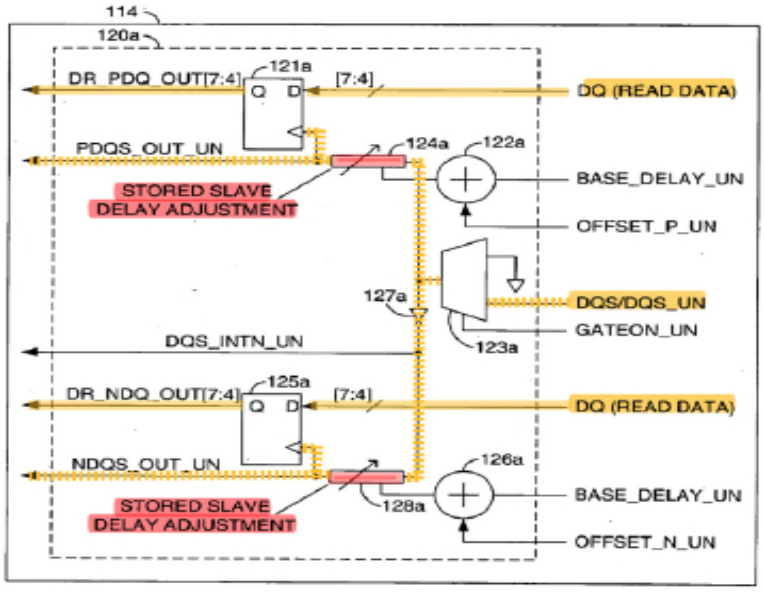


FIG. 3A

Id. Annotated Figures 2 and 3A of Butt, above, depict a "datapath," with element 114 of Figure 2 depicting a physical read datapath ("PHY DP") and

Figure 3A depicting a more detailed block diagram of datapath 114. Ex. 1029 ¶¶ 17, 25. As with the annotated versions of Figure 5 of Hiraishi, Petitioner depicts the alleged "data paths" of Butt's Figures 2 and 3A in orange highlighting. Pet. 36.

Additionally, Petitioner asserts that Hiraishi discloses a command processing circuit, i.e., "Data Register Control Circuit 320 and logic in DLL Circuit 310," configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal. Pet. 37 (citing Ex. 1003 ¶ 148).

For limitation 1[f], Petitioner asserts that Hiraishi discloses that the data path corresponding to each data signal line includes at least one tristate buffer, i.e. "output buffers OUTB and input buffers INB," controlled by the command processing circuit, and a delay circuit, i.e., "DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376," configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals. Pet. 39. Although Petitioner asserts that it is ambiguous as to whether the claim 1 language "in response to at least one of the module control signals" modifies the term "to delay" or the term "determined," Petitioner contends that the combination of Hiraishi and Butt discloses either interpretation. *Id.* at 43 (citing Ex. 1003 ¶ 155).

Petitioner also argues that Hiraishi discloses, with respect to the flow chart shown in Figure 13, a step "S4 Read/Write leveling to determine the delay through the data path." Pet. 41–42 (citing Ex. 1003 ¶ 152; Ex. 1005, Figs. 5, 13). Petitioner asserts that in a write leveling operation that is "performed during initialization in response to module control signals,"

where "[t]he write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS by displacing the internal clock LCLKW" such that "the phases of the clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other," "as shown in Figure 14B." *Id.* at 44–45 (quoting Ex. 1005 ¶¶ 145–146). Then, according to Petitioner, "data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 and performs a re-timing in synchronization with the phase-adjusted internal clock LCLKW which is used to read the FIFO circuit 301 to output the write data DQ and to generate the corresponding strobe DQS with Delay and Strobe Generating Circuits 370 and 374." *Id.* at 46 (citing Ex. 1003 ¶ 161; Ex. 1005 ¶¶ 84, 87, 91, 135, Fig. 5).

Petitioner additionally asserts, for write leveling operations, the alleged "delay circuit" includes

> Write FIFO 301 delaying the write data signal, delay circuit 370 delaying the LCLKW signal, the strobe generating circuit 374 generating a delayed strobe signal that is in synch with the delayed write data, and DLL circuit 310 generating the LCLKW signal for timing the output of the delayed data and strobe signals.

Pet. 47 (citing Ex. 1003 ¶ 161). Petitioner presents similar assertions with respect to the alleged "delay circuit" for read leveling operations, namely, that it includes

> FIFO (read) circuit 302 delaying the read data signal, delay circuit 372 delaying the input strobe signal, the strobe generating circuit 376 generating a delayed strobe signal that is in synch with the delayed read data, and DLL circuit 310 generating the LCLKR signal for timing the output of the delayed read data and strobe signals.

Id. at 51 (citing Ex. 1003 ¶ 166).

Patent Owner argues, and we agree, that Petitioner does not demonstrate that that Hiraishi teaches the recited "delay circuit" that delays a "signal thorough the data path." PO Resp. 28–40. Specifically, Patent Owner points to Petitioner's express disclosure that the "delay circuit" is the combination of Hiraishi's "DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376." PO Resp. 28 (citing Pet. 39, 47). Patent Owner contends, and we agree, that Dr. Wedig confirms that the combination including these components in Hiraishi are alleged to constitute the claimed "delay circuit." *See id*. at 28–29; Ex. 2012, 17:23–18:5 ("I believe that all of those different parts make up the delay circuit, so I guess yes, it's a combination of those. I mean, they all work together to implement the delay circuit.").

We also agree with Patent Owner that several of elements of Hiraishi alleged to be part of "a delay circuit" are not in a "data path" as claimed and do not "delay a signal through the data path." *See* PO Resp. 29–40. We refer to the data register buffer for write operations as shown in annotated Figure 5 of Hiraishi, reproduced below. *See* Pet. 34.

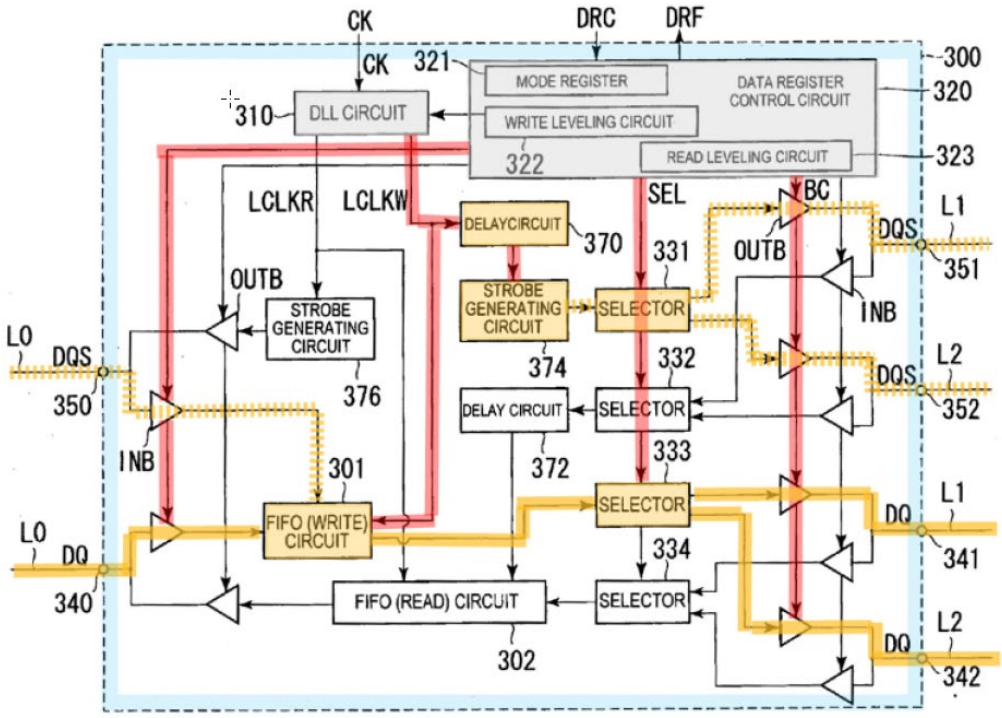


FIG.5

Annotated Figure 5 of Hiraishi, above, depicts the components of data register buffer 300, where Petitioner asserts that the "buffer circuit [300] including a data path" is shown in orange and "correspond[s] to each data signal line in the respective set of data/strobe signal lines [L0, including lines DQ (data) and DQS (strobe) . . .". Pet. 33 (emphasis omitted); Ex. 1005 ¶¶ 83–84.

Patent Owner contends that several components of the alleged "delay circuit" as shown in the data register buffer for write operations are not in the "data path" and do not "delay a signal through the data path." Pet. 29–36. Specifically, Patent Owner refers to delay circuit 370, which Petitioner contends is part of the claimed "delay circuit," and argues that that the local clock signal LCLKW to delay circuit 370 is not "a signal through the data path." As noted above, Petitioner identifies the paths shown in orange as the

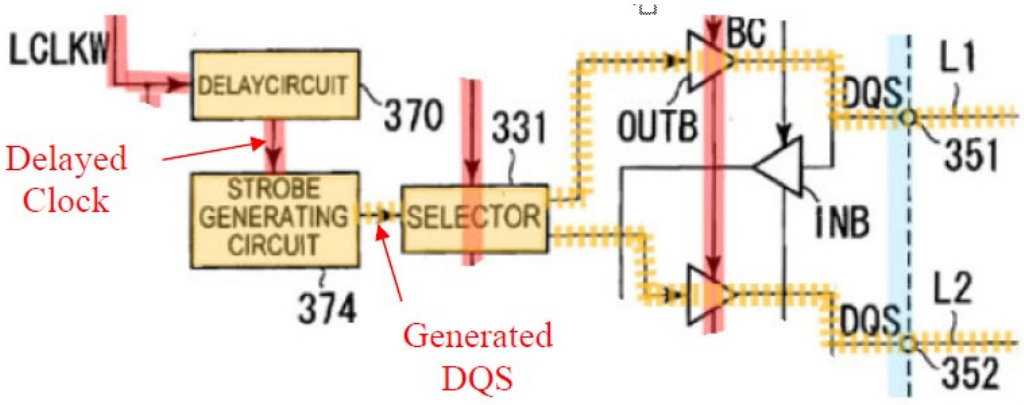
claimed "data path" as shown in annotated Figure 5 of Hiraishi. *See* Pet. 33–34. Patent Owner asserts, and we agree, that the LCLKW signal to data circuit 370 does not travel on an orange line, and is therefore not through the "data path," as mapped by Petitioner. *See* PO Resp. 31–32. This is confirmed by Dr. Wedig's testimony:

> Q. How about the red -- I guess red lines? Are those part of the data path?
>
> A. No, they're not. They're not part of the data path.
>
> . . .
>
> Q. How about the CLK signals LCLKR and LCLKW, are those part of the data path through Hiraishi's data buffer?
>
> A. No. They're not.

Ex. 2012, 41:2–5, 42:1–4.

Accordingly, the evidence of record does not support that the LCLKW signal to delay circuit 370 is through the "data path" as claim 1 requires.

Patent Owner also asserts, and we agree, that strobe generating circuit 374, alleged to be part of the recited "delay circuit," is not in the data path. PO Resp. 32–33. Patent Owner refers to an enlarged annotated portion of Figure 5, reproduced below. *Id.* at 33–34.



Above is an annotated expanded version of a portion of Hiraishi's Figure 5 in the area around strobe generating circuit 374. PO Resp. 33–34. As discussed above, claim 1 requires that the recited "data path" correspond to data signal lines carrying data signals, not to strobe signal lines carrying strobe signals. As shown, strobe generating circuit 374 receives a clock signal, which is not on the "data path" as mapped by Petitioner, and sends a strobe signal to selector 331, which is not on a "data path" as claimed, that is, on a "data signal line in the respective set of data/strobe signal lines." *See id*. at 33; Ex. 2013 ¶ 94.

According, the evidence of record does not support that strobe generating circuit 374 of Hiraishi, which Petitioner alleges is part of the claimed "delay circuit" is in the "data path" as claim 1 requires.

Patent Owner further asserts, and we agree, that Hiraishi's DLL circuit 310 is not in the "data path" of claim 1, nor does it delay "a signal through the data path." *See* PO Resp. 34–36. As shown in the annotated version of Figure 5 of Hiraishi, DLL circuit 310 is not in the "data path," the orange path. This is confirmed by Dr. Wedig. Ex. 2012, 42:24–43:1 ("Q. Is the DLL circuit 310 part of the data path through Hiraishi's data buffer? A. No, it's not."). As Patent Owner also contends, neither the CK signal to DLL circuit 330 nor the LCLKW output are "a signal through the data path" because Petitioner does not identify these signal lines as part of the claimed "data path" as shown in Figure 5. *See* PO Resp. 35–36. Dr. Wedig confirms this. *See* Ex. 2012, 41:2–25, 42:1–4.

Accordingly, the evidence of record does not support that DLL circuit 310 of Hiraishi, which Petitioner alleges is part of the claimed "delay circuit," is in the "data path" as claim 1 requires, nor does the CK signal to DLL circuit 330 nor the LCLKW output "signal[s] through the data path."

We also refer to the data register buffer for read operations as shown in annotated Figure 5 of Hiraishi, reproduced below. *See* Pet. 34.

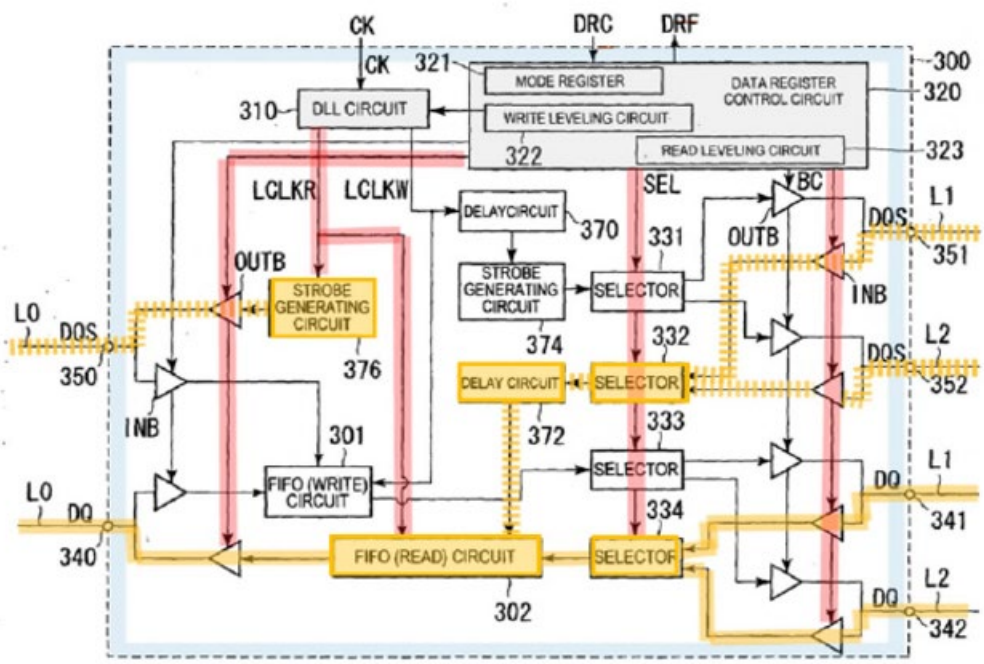


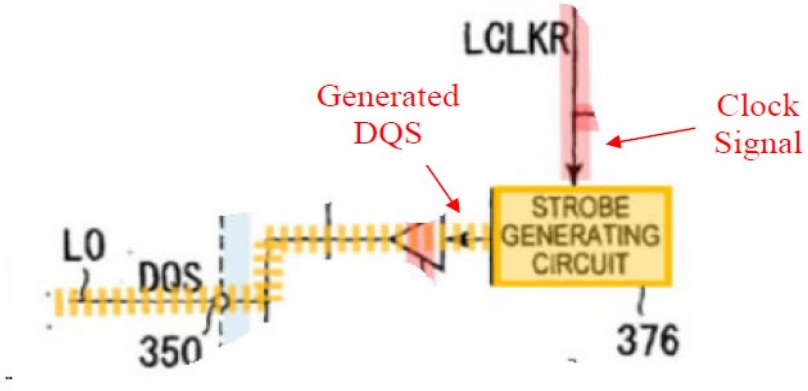
FIG.5

Annotated Figure 5 of Hiraishi, above, depicts the data register buffer, with Petitioner asserting that the "buffer circuit [300] including a data path" is shown in orange and "correspond[s] to each data signal line in the respective set of data/strobe signal lines [L0, including lines DQ (data) and DQS (strobe) . . .". Pet. 33 (emphasis omitted); Ex. 1005 ¶¶ 83–84.

Patent Owner asserts, and we agree, that Hiraishi's delay circuit 372 is not in a data path and does not delay "a signal through the data path" as required by claim 1. PO Resp. 37–38. Again, as discussed above, claim 1 requires that the recited "data path" correspond to data signal lines carrying data signals, not to strobe signal lines carrying strobe signals. As shown in annotated Figure 5, delay circuit 372 is in a strobe path (i.e., depicted in orange broken line vs. orange solid line) and is not in a path carrying data signal lines. *See* Ex. 2013 ¶ 104. Accordingly, the evidence of record does

not support that delay circuit 372 of Hiraishi, which Petitioner alleges is part of the claimed "delay circuit," is in the "data path" as claim 1 requires.

Patent Owner also asserts, and we agree, that Hiraishi's strobe generating circuit 376 is not in the "data path" as claimed. PO Resp. 38–39. Patent Owner refers to an enlarged annotated portion of Figure 5, reproduced below. *Id*. at 39.



Above is an annotated expanded version of a portion of Hiraishi's Figure 5 in the area around strobe generating circuit 376. PO Resp. 38–39. As discussed above, claim 1 requires that the recited "data path" correspond to data signal lines carrying data signals, not to strobe signal lines carrying strobe signals. As shown, strobe generating circuit 376 receives a clock signal LCLKR, which is not on the "data path" as mapped by Petitioner, and sends a strobe signal, which is not on a "data path" as claimed, that is, on a "data signal line in the respective set of data/strobe signal lines." *See id*. at 38–39; Ex. 2013 ¶ 105.

Accordingly, the evidence of record does not support that strobe generating circuit 376 of Hiraishi, which Petitioner alleges is part of the claimed "delay circuit," is in the "data path" as claim 1 requires.

Thus, for the reasons discussed above, Petitioner fails to demonstrate that Hiraishi teaches or suggests the "delay circuit" of claim 1.

Petitioner relies only on the mapping of elements to Hiraishi for the teaching of the "data path" that includes the "delay circuit," and not Butt for teaching the claimed "delay circuit." Pet. 33–34, 39–51. We note that Petitioner makes some assertions related to Butt, but they do not indicate that specific elements of Butt are relied upon or combined to Hiraishi for the teaching of the "delay circuit." For instance, Petitioner refers to Butt's "circuit between a memory controller and DDR memory devices uses strobe signals to sample the data signals and buffers the data samples in FIFOs." *Id*. at 35. But Petitioner does not rely upon Butt for teaching the "data path" that includes the "delay circuit" as claimed. *Id*. at 36. Instead, Petitioner generally asserts that a person of ordinary skill in the art "would have understood from the disclosure of Butt that Hiraishi's data register buffer 300 includes 'data paths.'" *Id*. (emphasis omitted). The Petition also makes the statement that that a person of skill "would have been motivated to implement Butt's data path controlling technique in Hiraishi's data register buffer." *Id*. at 39–40 (citing Ex. 1003 ¶ 152; Ex. 1005, Fig. 5. (emphasis omitted). However, although the Petition and Dr. Wedig's testimony refer to Butt for its "data path techniques," only Hiraishi's Figure 5 is relied upon for the teaching of "data path[s]." *See* Pet. 39–51; Ex. 1002 ¶¶ 144–147, 152. The Petition, therefore, does not rely on Butt for teaching the "data paths" or "delay circuit" of claim 1; Hiraishi only is relied on.

Thus, considering the evidence and arguments presented in the Petition, Petitioner has not shown by a preponderance of the evidence that claim 1 is unpatentable over Hiraishi and Butt.

4. Discussion of the Revised Contentions and Evidence of Petitioner's Reply and Associated Patent Owner Responses in Sur-reply

As we noted above, Petitioner presented argument and evidence under

its original assertions in the Petition. In the Petition, Petitioner asserted that the delay circuit is the "DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376." Pet. 39. In Reply, Petitioner revised its assertions based on Hiraishi, asserting that a different signal line to/from Hiraishi's FIFO circuit 302 is the claimed "delay circuit" on the "data line" in accordance with Figure 16 of the '608 patent, that is, that each of the respective read/write FIFO circuits is the claimed "delay circuit." *See* Pet. Reply 12–15. Petitioner's revised mapping in Hiraishi of the alleged "data path" in the Reply is reproduced in annotated Figure 5 below. *Id.* at 14.

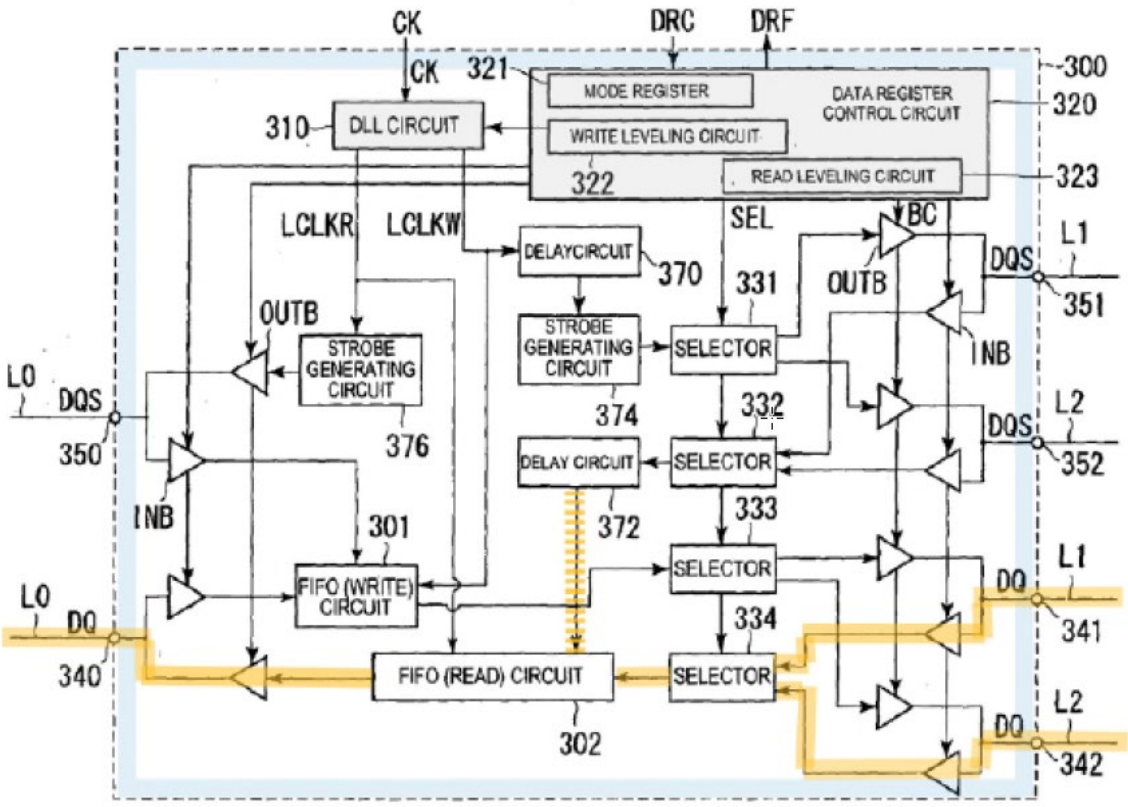


FIG.5

Annotated Figure 5, above, depicts Petitioner's revised mapping of the alleged "data path" in Hiraishi. Pet. Reply 14. In Reply, Petitioner contends

that the DQ data signal lines, in solid orange, directly correspond to the "delay circuit" on the "data path," under Patent Owner's interpretation of the claim term "data path." *Id.* at 13. Petitioner presents related arguments as to why Hiraishi's FIFO teaches all the limitations for the claimed "delay circuit," including that it delays the signal by an amount determined by the command processing circuit in response to module control signals. *Id.* at 16–32.

Also, in Reply, Petitioner refers to the assertion in the Petition that a person of skill "would have been motivated to implement Butt's data path controlling technique in Hiraishi's data register buffer." Pet. Reply 16 (citing Pet. 33–41; Ex. 1029, Figs. 2, 3; Ex. 1074, 181:19–183:1, 184:1–190:7, 199:2–200:2, 201:14–202:5; Ex. 1084, Figs. 2, 3, 14) (emphasis omitted). Although Petitioner refers to a statement in the Petition, several of citations noted in Reply are not cited in the Petition, e.g., the citations to Exhibits 1074 and 1084. *Id.*

We first address if we should consider Petitioner's arguments newly-presented in Reply.

a. Newly-Raised Arguments in Petitioner's Reply

A petitioner may reply to arguments raised by patent owner in its response, but may not raise "in reply, 'an entirely new theory of *prima facie* obviousness absent from the petition,' even if the new theory is responsive to the patent owner's response or the Board's institution decision." *Corephotonics, Ltd. v. Apple Inc.*, 84 F.4th 990, 1008 (Fed. Cir. 2023) (quoting *Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.*, 853 F.3d 1272, 1286 (Fed. Cir. 2017)).

Patent Owner objects to Petitioner's new arguments and evidence presented in Reply as improper. PO Sur-reply 7–8. At the oral hearing,

Patent Owner referred to its footnote in its Preliminary Response stating that the delayed signal is the DQ signal, not the DQS signal, which Patent Owner states was not a "fully fleshed out claim construction position." *See* Tr. 47:21–48:5 (referring to Prelim. Resp. 10, n.2). Patent Owner contends that Petitioner had the opportunity to respond in a preliminary reply to Patent Owner's Preliminary Response, and did not do so. *See id*. At the oral hearing, Petitioner argued that the new arguments in its Reply are proper because Patent Owner raised claim construction issues in its Response and its arguments are in response to the new claim construction issues. *See id*. at 11:26–12:8, 15:18–22 (referring to *Axonics, Inc. v. Medtronic, Inc*., 75 F.4th 1374 (Fed. Cir. 2023)). Petitioner further argued that Patent Owner changed its theories on claim interpretation from that presented in litigation against Petitioner, which Patent Owner disputes. *Id*. at 48:14–24, 55:3–15.

In *Axionics*, the Federal Circuit held that when a patent owner offers a new claim construction for the first time in its response after the institution decision, a petitioner may introduce new arguments and evidence in reply under the newly proposed claim construction. *Axonics*, 75 F.4th at 1380–81, 1384. We find this to be a close issue under the particular circumstances here because, as discussed above, in our view this is a case where the language of claim 1 of the '608 patent is dispositive of how the claim term "data path" should be interpreted. Nonetheless, Patent Owner admits that its position on the interpretation was not fully developed in its Preliminary Response (Tr. 47:25), and Patent Owner's Response presented more detail on its interpretation of the claim (PO Resp. 18–24). Accordingly, under *Axonics*, we will consider Petitioner's newly-raised evidence and argument in Reply.

b. Analysis of Newly-Raised Arguments in Petitioner's Reply

i. Claim 1

In Reply, Petitioner asserts that the DQ data signal lines, in solid orange on the signal lines associated with Hiraishi's FIFO Read Circuit 302, directly correspond to the "delay circuit" on the "data path," under Patent Owner's interpretation of the claim term "data path," as this is consistent with Figure 16 of the '608 patent. Pet. Reply 13–14. Annotated Figure 5 of Hiraishi and annotated Figure 16 of the '608 patent are reproduced below.

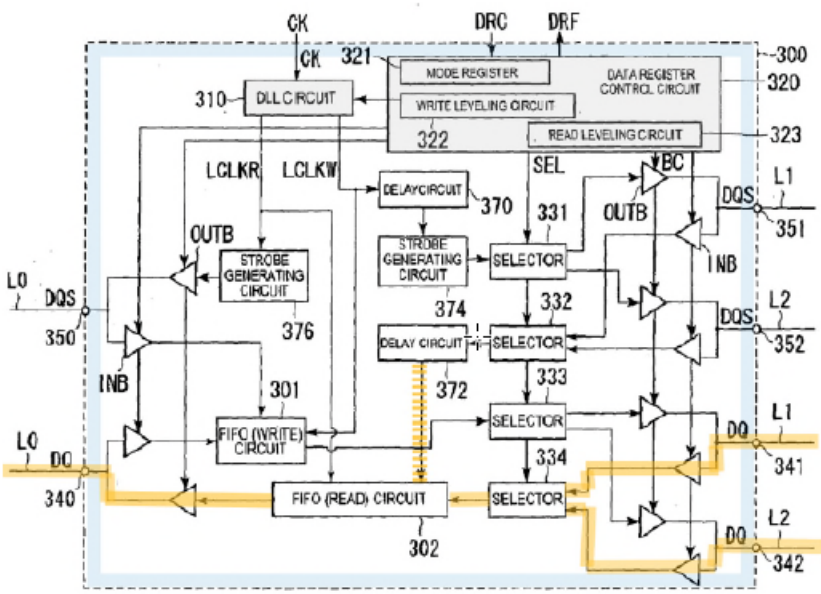


FIG.5

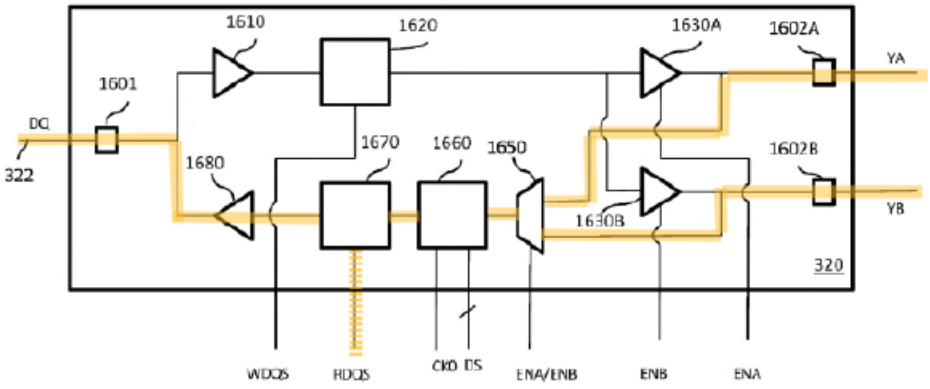


FIG. 16

Annotated Figure 5, above, depicts Petitioner's revised mapping of the alleged "data path" in Hiraishi and Petitioner's annotated Figure 16 of the '608 patent is a DQ routing circuit with a delay circuit in a data buffer. Pet. Reply 14; Ex. 1001, 3:14–15. Petitioner highlights in orange solid line the alleged "data path" in both figures.

Petitioner argues that Hiraishi's Figure 5 "matches" Figure 16 of the '608 patent in the write direction. Pet. Reply 14. Petitioner also presents arguments as to why Hiraishi's FIFO teaches all the limitations for the claimed "delay circuit." *Id.* at 16–32.

The main issue in dispute is whether Hiraishi teaches the claimed "delay circuit" that "delays a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals." *See* Pet. 43–53; Pet. Reply 12–32; PO Resp. 40–58; PO Sur-reply 9–18.

Petitioner asserts that "Hiraishi's Read FIFO 302 is on the DQ data line and delays the DQ data signal," and this is also true for the write direction. Pet. Reply 15 (citing Pet. 48–53; Ex. 1005 ¶¶ 130, 135) (emphasis omitted). Petitioner argues that there is a two-step process in Hiraishi that teaches the delay of a signal as claimed in limitation 1[f]. Petitioner contends that during initialization "the DRC signal causes the Data Register Control Circuit 320 to perform S4 read/write leveling, which determines and stores the variable amount of delay needed." *Id.* at 18 (citing Ex. 1005, Figs. 14, 15) (emphasis and footnote deleted). Petitioner argues that this delay is not "fixed," as asserted by Patent Owner, because it varies depending on the "flight time" of the data and strobe signals. *Id.*, n.4. More specifically, Petitioner asserts that the S4 read/write leveling determines a variable

amount of delay is needed "because data line L1 to the upper memory chip is longer than data line L2 to the lower memory chip." *Id.* at 20–21 (citing Pet. 31–32; Ex. 1005 ¶¶ 55, 56, Fig. 1). Petitioner argues that Patent Owner's expert conceded that the flight time for L1 will be greater than that of L2. *Id.* at 21 (Ex. 1074, 208:3–15, 210:24–211:22, 217:2–16, 223:20–224:4). Petitioner asserts that in the second step, during "normal operation," for example, "in response to a read/write command transmitted via DRC . . . , that stored delay amount [from levelling] is used to control the '*delay circuit*' to delay (i.e., "retim[e]") both the DQ data signals (e.g., using the FIFOs 301/302) and the DQS strobe signals associated with that normal read/write command," as shown in Hiraishi at Figures 11 and 12. *Id.* at 18–19 (citing Pet. 37–51; Ex. 1070 (Figs. 11, 15); Ex. 1071 (Fig. 14); Ex. 1081 (Fig. 12)).

Patent Owner makes several arguments as to why Hiraishi's FIFO circuits do not teach the "delay circuit" of limitation 1[f] under the revised contentions. PO Sur-Reply 9–18.

We note that Petitioner did not submit an expert declaration in further support of its Reply; Petitioner relies only on the Wedig Declaration that was submitted with its Petition (Ex. 1003). As discussed above, the Petition and Dr. Wedig relied on the combination of Hiraishi's DLL 310, FIFOs 301/302, delay circuits 370/372, and strobe generating circuits 374/376 as the "delay circuit" for claim 1. *See* Pet. 39; PO Sur-reply 8; Ex. 1003 ¶ 152; Ex. 2012:17:23–18:5. There is no declaratory expert testimony in the record, therefore, in support of Petitioner's new assertion in Reply that only Hiraishi's FIFO circuits teach the claimed "delay circuit." *See* Pet. Reply 12–32.

In Reply, one of Petitioner's arguments is that obviousness is based on similarities of Hiraishi to Figure 16 of the '608 patent. Pet. Reply 12–15. We do not agree. More specifically, Petitioner asserts that, regardless of the construction of the term "data path," "Figure 5 [shown on p. 14 of Petitioner's Reply] renders obvious that claim language because it is substantially identical to Figure 16 of the '608 Patent, which Netlist admits embodies the claim language." *Id.* at 14–15 (citing PO Resp. 27). Figure 16 of the '608 patent, however, differs from Hiraishi in that Figure 16 of has a delay circuit 1660, which receives a "delay signal DS," as Patent Owner asserts. *See* PO Sur-reply 9 (citing Ex. 1001, 10:31–35, 17:48–56, Fig. 3). As Patent Owner notes, the buffer circuit of the '608 patent includes a circuit 1670 that samples the delayed read signal, whereas Hiraishi uses a delayed strobe signal from delay circuit 372 to sample non-delayed data in FIFO 302. *Id.* (citing Ex. 1001, 17:56–60; Ex. 1005 ¶¶ 84, 91,[12] Fig. 5). Accordingly, we do not find that any facial similarities of Figure 16 of the '608 patent and a portion of Figure 5 of Hiraishi lead to a conclusion that Figure 5 "embodies the claim language" in view of the differences in the respective details and functions of the two systems. *See id.* As is discussed below, the relevant issue is instead whether Petitioner carries its burden to demonstrate that the evidence and argument presented in Reply show that the prior art teaches the "delay circuit" of claim 1.

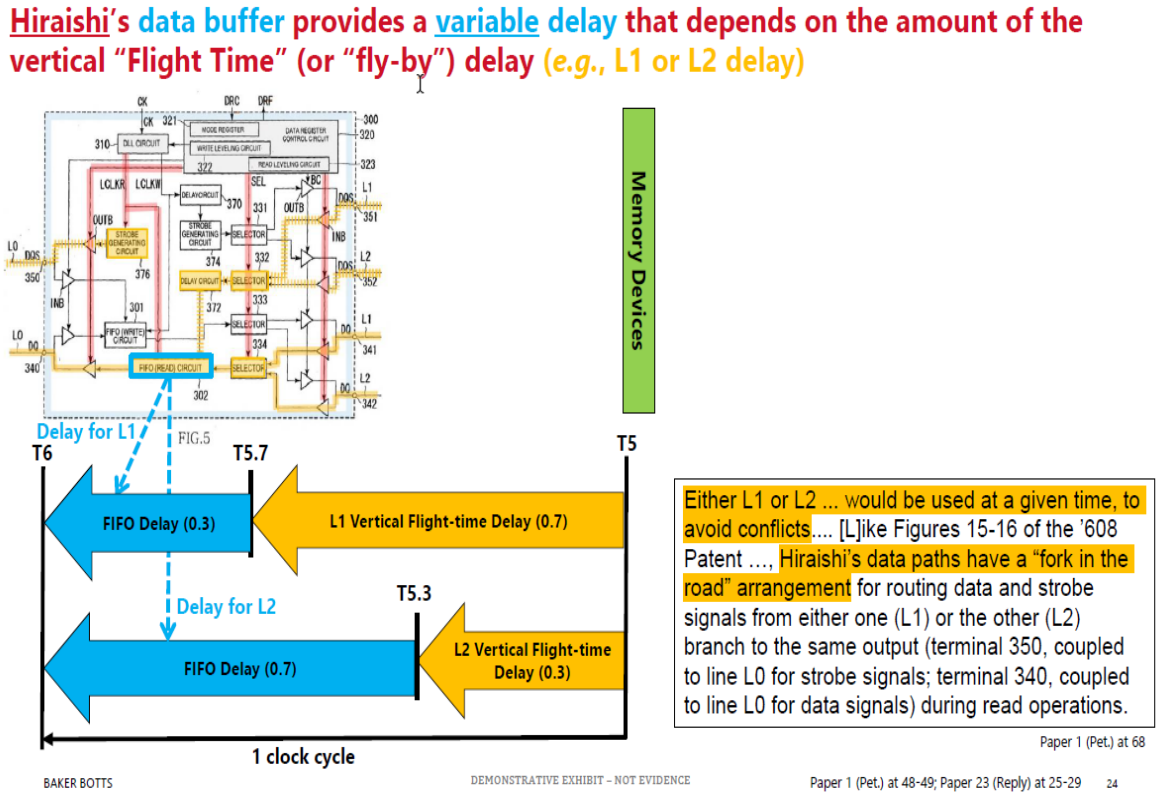
Petitioner also argues that the Board's findings in the -00236 IPR "bind" us to concluding that "Hiraishi teaches 'controlling the timing of data and strobe signals on the data paths' as part of read and write leveling in

[12] Patent Owner cites to paragraph 92 of Hiraishi, which does not discuss delay circuit 372. This appears to be a typographical error and the correct citation is paragraph 91.

response to the 'DRC' module control signal." Pet. Reply 12–13 (citing Ex. 1066, 35–36, 52) (emphasis omitted). We do not agree. As discussed in the Final Written Decision in the -00236 IPR, the Board found that in Osanai the data register control circuit 320 selects certain paths using SEL, INB, and OUTB signals, which are sent to selectors 331–334 and INB/OUTB buffers (Ex. 1066, 19, 24, 26), whereas, in the instant proceeding, Petitioner relies on Hiraishi's INB/OUTB buffers and the signals sent there for the tristate buffer limitation (Pet. 42), and Petitioner does not argue that selectors 331–334 or that the INB/OUTB buffers delay a signal (*see* Pet. 43–51; Pet. Reply 12–32) .

As noted above, Petitioner alleges that there is a two-step process in Hiraishi that teaches the delay of a signal and the amount of time for the delay, where the first step is during initialization where "the DRC signal causes the Data Register Control Circuit 320 to perform S4 read/write leveling, which determines and stores the variable amount of delay needed." Pet. Reply 18 (citing Ex. 1005, Figs. 14, 15) (emphasis and footnote omitted). Petitioner argues that "[t]he delays measured by S4 read/write leveling are then 'stored' in Data Register Control Circuit 320 for future use by the '*delay circuit*' during normal operations." *Id*. at 23 (citing Ex. 1005 ¶¶ 146, 151; Pet. 45–46, 49–50). Petitioner asserts that in the second step, during 'normal operation," for example, "in response to a read/write command transmitted via DRC, that stored delay amount is used to control the '*delay circuit*' to delay (i.e., "retim[e]") both the DQ data signals (e.g., using the FIFOs 301/302) and the DQS strobe signals associated with that normal read/write command." *Id*. at 18–19 (citing Pet. 37–51; Ex. 1070, Figs. 11, 15; Ex. 1071, Fig. 14; Ex. 1081, Fig. 12). Petitioner asserts that this two-step process is needed in Hiraishi "because data line L1 to the upper

memory chip is longer than data line L2 to the lower memory chip." *Id.* at 20–21 (referring to Ex. 1005, Fig. 1 with lines L1 and L2 located between buffers and memory chips). At oral hearing, Petitioner presented a slide depicting the alleged two-step process, which is reproduced below.



Ex. 1089, slide 24.

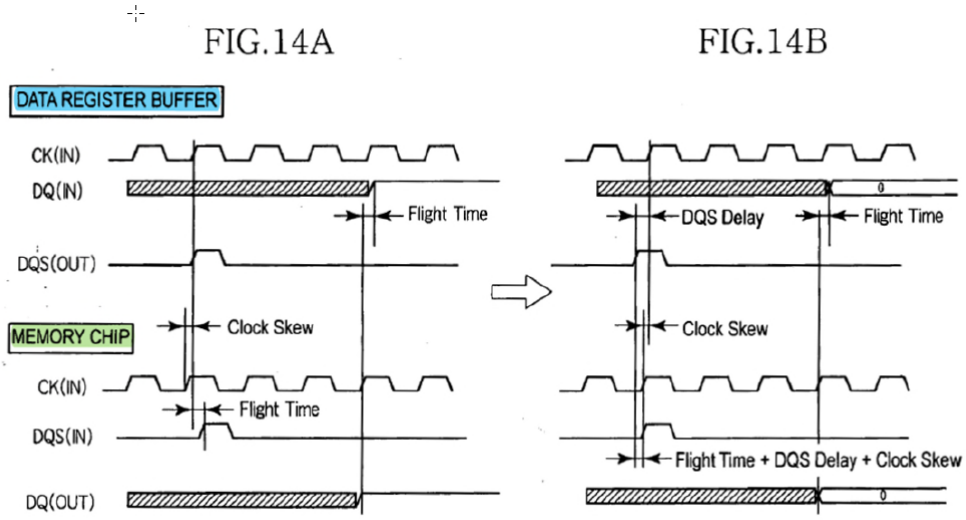
We consider the issue of Hiraishi's teachings of a "delay circuit" that delays "a signal through the data path by an amount determined . . . in response to at least one of the module control signals," and evaluate Petitioner's assertions as to Hiraishi's S4 read/write leveling, with write leveling and read leveling considered separately, as well as whether any alleged stored "delay amount" would be used in the alleged second step of retiming.

Petitioner asserts that Hiraishi's FIFOs 301/302 delay the data signal by an amount determined by the command processing circuit "in response

to" "the module control signal." Pet. 20–21, 44–47; Pet. Reply 16–19. Petitioner argues that the module control signals include DRC. *See* Pet. 20–21 (citing Ex. 1005, Fig. 7 (on control line L4)); Pet. Reply 16–18.

The Petition contends that "Hiraishi's data register buffer 300 *determines delays through the data path for read and write operations by respective read and write leveling operations during initialization* in response to control signals from the command/address/control register 400, *and applies those delays on the data/strobe signals for read and write operations*[13] *during normal operation* in response to read and write commands received from the command/address/control register 400." Pet. 43–44 (emphasis added). Specifically, Petitioner asserts that during S-4 initialization (leveling) step, the DRC conveys "mode switching" or "mode register set" commands by a write leveling circuit 322 "to adjust a write timing . . . in consideration of a propagation time of a signal." Pet. 44–45 (citing Ex. 1003 ¶ 159; Ex. 1005 ¶¶ 88, 90, 100, 140, 142, Fig. 5); *see also id.* at 53–54 (citing Ex. 1005 ¶¶ 139–140; Ex. 1003 ¶¶ 159–160, 172–174, 176; Ex. 1020, 29, 31, 33, 43, 48–54[14]); Pet. Reply 17–18. The Petition contends that "[i]n response to a write leveling mode register set command, the memory devices provide feedback of a local clock sampled by the strobe signal, and the write leveling circuit 322 is activated by corresponding DRC signals to process that feedback." Pet. 45 (citing Ex. 1020 (JESD79-3C), 42–43). Petitioner refers to Figures 14A and 14B of Hiraishi, as reproduced below (*Id.* (citing Ex. 1003 ¶ 160; Ex. 1005 ¶¶ 142–146)).

[13] We also refer to the read and write operations of Hiraishi as "retiming."
[14] JEDEC DDR3 SDRAM Standard, JESD79-3C (April 2008).



Pet. 45. Figures 14A and 14B of Hiraishi, above, depict timing charts explaining the write leveling operation between the data register buffer 300 and the memory chip 200, with Figure 14A showing a timing chart at the time of starting the leveling, and Figure 14B is a timing chart at the end of leveling. Ex. 1005 ¶ 27. Petitioner asserts that "Figure 14A shows that, before write leveling, the strobe signal DQS is off from the memory's local clock." Pet. 45. Petitioner refers to Hiraishi's disclosures that "'[t]he write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS by displacing the internal clock LCLKW' such that 'the phases of the clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other.'" *Id.* (citing Ex. 1005 ¶¶ 145–146). Petitioner contends that "[t]he delays determined during write leveling are stored in the data register buffer 300 and applied by the control circuit 320 to delay both the data and data strobe signals during subsequent write operations to ensure that the standard data to strobe timing requirements are met at the memory devices," referring to Figure 12. *Id.* at 45–46 (citing Ex. 1005, Fig. 15; Ex. 1003 ¶ 160; Ex. 1020, 68). Dr. Wedig testifies that "[a] Skilled Artisan would have understood that

delaying both the data and strobe signals ensures that the standard data to strobe timing requirements are met at the memory devices." Ex. 1003 ¶ 160 (citing JESD79-3C (Ex. 1020), 68). Petitioner then contends that "Hiraishi's data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 and performs a re-timing in synchronization with the phase-adjusted internal clock LCLKW." Pet. 46 (citing Ex. 1003 ¶ 161; Ex. 1005 ¶¶ 135, 87, 84, 91, Fig. 5).

In Reply, Petitioner asserts that Hiraishi teaches write leveling performed during initialization in response to the claimed module control signals as "*e.g., DRC* conveying 'mode switching' or 'mode register set' commands)." Pet. Reply 17 (citing Pet. 44–47). Petitioner refers to the Petition at pages 48–51 for similar teachings on read leveling. *Id*. Petitioner asserts that a Mode Register Set (MRS) command was "the standard command initialization." *Id*., n.3 (citing Ex. 1074, 104:21–107:8; 119:20–123:7, 123:8–128:21, 79:23–80:14, 89:6–90:9; Ex. 1020, 26, 42, 31, 48, 50–51; Ex. 1085, 7, 9). In support of the Petition, and relating to claim 2, Dr. Wedig testifies that:

> A Skilled Artisan would have understood that a '*first set of command signals'* [claim 2] from the memory controller is also necessary for the S4 read/write leveling operation ('*first memory operation*' under Netlist's interpretation). For example, Hiraishi discloses that the 'initializing operation includes a mode register setting operation by which predetermined mode information is set in the mode registers 215, 321, and 431 that are included in the memory chip 200, the data register buffer 300, and the command/address/control register buffer 400, respectively (Step S3). Upon completing the mode register setting operation, a leveling operation between the data register buffer 300 and the memory chip 200 is performed (Step S4).' Hiraishi at [0139-40]. A Skilled Artisan would have understood from this disclosure that the system memory controller instructs the

> command/address/control register buffer on Hiraishi's module to perform the S4 read/write leveling using 'a first set of command signals,' similar to the mode switching commands and mode register set commands for read and write leveling in the memory devices. *See, e.g.*, EX1020 (JESD79-3C) at 31, 33, 48–54 (multipurpose register for read calibration), 43 (mode register setting for write leveling); *see also supra* at ¶¶ 159–160.

Ex. 1003 ¶ 176.

We agree with Patent Owner that Petitioner fails to demonstrate that Hiraishi teaches that the delays determined by S4 write and read leveling are then used to determine delays through the data path for read and write operations. *See* PO Resp. 41–46; PO Sur-reply 6, 13–18; Ex. 2013 ¶¶ 110–115. Below we first address issues predominantly relating to Hiraishi's write leveling, and then turn to read leveling.

In the Petition's discussion of the write leveling process during initialization in Hiraishi, Petitioner asserts that "*[t]he delays determined during write leveling are stored* in the data register buffer 300 and applied by the control circuit 320 *to delay both the data and data strobe signals during subsequent write operations*," as discussed above. Pet. 45–46 (emphasis added). Based on the evidence of record, we do not agree. Hiraishi's write leveling is done to address mismatches between the time of receipt of the clock signal CK and the data strobe signal DQS at memory chip 200. That is, write leveling is not done to determine delays in data signal lines to account for different flight time delays for L1/L2, as Petitioner asserts. *See* Tr. 10:6–14, 11:1–3; Ex. 1089, slides 20, 24. This is consistent with Hiraishi's disclosures. Ex. 1005 ¶¶ 142–146; Figs. 14A, 14B; Ex. 2013 ¶¶ 110–111. For instance, Hiraishi discloses:

> *In the write leveling operation between the data register buffer 300 and the memory chip 200*, as shown in FIG. 14A, the data

> register buffer 300 outputs *a data strobe signal DQS that is synchronized with the clock signal CK*.
>
> . . .
>
> Upon completing the write leveling operation in this manner, the phases of the *clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other*.

Ex. 1005 ¶¶ 142, 146 (emphasis added). Dr. Mangione-Smith provides supporting testimony that Hiraishi's S4 write leveling is for aligning the DQS signal to the system clock signal CK for input to the memory chip. Ex. 2013 ¶¶ 109–110. We credit this testimony because it is consistent with Hiraishi's disclosures. Dr. Wedig also agrees that Hiraishi's S4 write leveling is used to address mismatches between the clock signal CK and the data strobe signal DQS. Ex. 2012, 60:7–12 ("So what happens in S4 write leveling -- we are now looking at the relationship between the CLK and the DQS signal that appears at the input to the memory device. We want that to now be in synch.").

The parties have different views of how Hiraishi operates. As noted above, Petitioner contends that delays determined during write leveling are stored and used during subsequent re-timing operations. *See* Pet. 43–46; Ex. 1003 ¶¶ 166–167; Pet. Reply 16–17. In contrast, Patent Owner argues that write leveling is a separate process that adjusts the timing of DQS to align with the clock, and the re-timing step is not based on write leveling. PO Resp. 41–46; PO Sur-reply 13–18; Ex. 2013 ¶¶ 110–115. Patent Owner further asserts that re-timing for writing is independently done by re-timing the latency period (CL/WL) to the next higher clock cycle. PO Resp. 46–58; PO Sur-reply 13–18; Ex. 2013 ¶¶ 116–131.

Petitioner has the burden to demonstrate that Hiraishi teaches that the two-step method where delays in write leveling during initialization is

applied to the retiming write operation during normal operation. Here, we find that the weight of evidence does not support Petitioner's assertion.

Patent Owner refers to several disclosures in Hiraishi to support that write leveling is a separate step than re-timing used in the write operation. As discussed above, the evidence of record supports that Hiraishi's S4 write leveling is directed to aligning the DQS signal to the system clock signal CK. As Patent Owner asserts, Hiraishi discloses that "[u]pon completing the write leveling operation in this manner, the phases of the clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other." PO Resp. 43 (citing Ex. 1005 ¶ 146). Patent Owner refers to Hiraishi's description and depiction that there is an "initializing operation" as shown in Figure 13, reproduced below, and that Figure 12 is a separate "writing operation," where "a normal write operation [] occurs ***after*** Hiraishi performs its write leveling during initialization." *Id*. at 44 –45 (citing Ex. 1005 ¶ 138 ("FIG. 13 is a flowchart for explaining the *initializing* operation of the memory module 100 at the time of activation.") (emphasis added), Figs. 12, 13); *see also* Ex. 2013 ¶ 113.

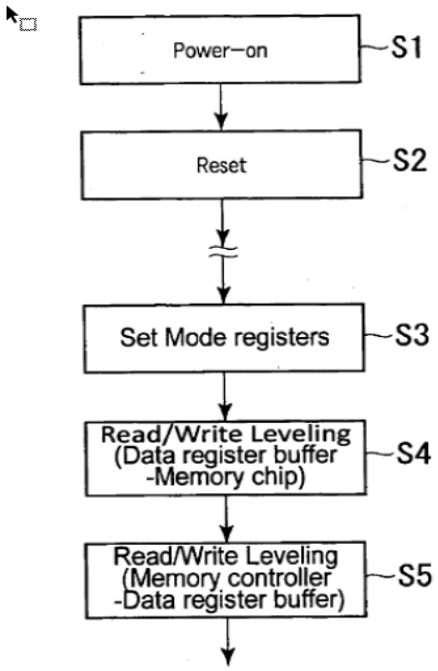


FIG.13

Figure 13, above, is a flowchart for explaining the initializing operation of the memory module. Ex. 1005 ¶¶ 26, 138.

Dr. Mangione-Smith testifies that in the S4 write leveling, the clock (CK(IN)) signal and strobe (DQS(IN)) signal are aligned as shown in red in Figure 12, reproduced below. Ex. 2013 ¶ 114.

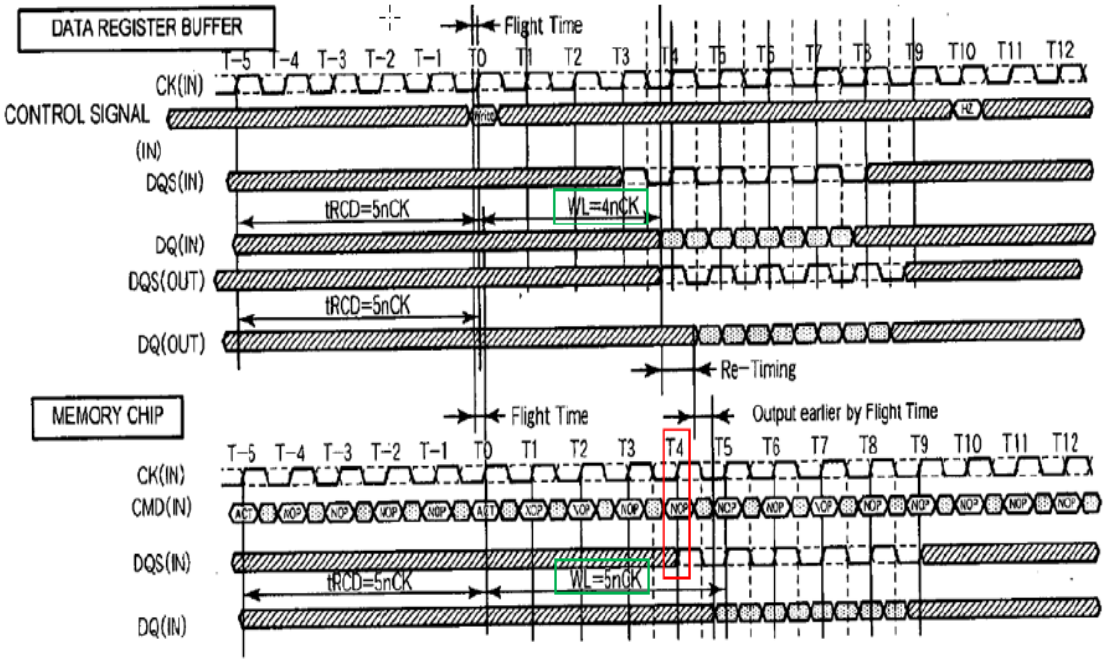


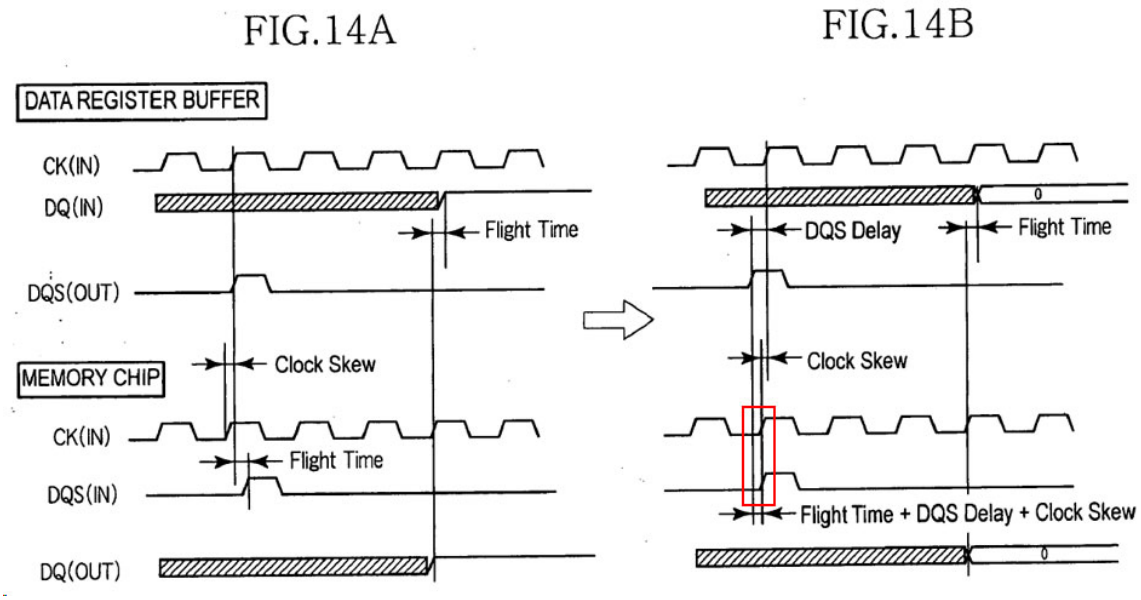
FIG.12

Figure 12, above, depicts a timing chart for explaining the write operation of the memory module 100. Ex. 1005 ¶ 25. Dr. Mangione-Smith further refers to Figure 12 above and testifies that "the DQ data re-timing from a write latency of 4 clock cycles (WL=4) to a write latency of 5 clock cycles (WL=5) is indicated as a distinct occurrence (highlighted in green)." Ex. 2013 ¶ 114. Dr. Mangione-Smith testifies that "I do not agree that Hiraishi's S4 write leveling relates to delaying data in a data path, or that the results of S4 write leveling are used to [] carry out Hiraishi's WL re-timing." *Id.* ¶ 115.

Dr. Wedig provided testimony on this issue, stating that the "resulting delays" of S-4 write leveling "*are stored in the data register buffer 300 and applied to delay both the data and data strobe signals during subsequent write operations* such that both write data and strobe signals arrive at the memory with a predetermined latency WL=5." Ex. 1003 ¶ 160 (emphasis added) (referring to Figure 12 of Hiraishi). As

discussed above, Dr. Mangione-Smith does not agree that a person of skill in the art would understand Hiraishi's disclosures to mean that. Ex. 2013 ¶ 112. Instead, Dr. Mangione-Smith testifies that:

> However, Hiraishi states that the 'result of the write leveling operation is stored in the data register control circuit 320 in the data register buffer 300,' and that '[u]pon completing the write leveling operation in this manner, the phases of the clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other.' EX1005, [0146]. *A POSA [person of ordinary skill in the art] would understand this passage to mean that the result of Hiraishi's write leveling which is stored is not used to delay data and data strobe signals during subsequent write operations, but instead is used to delay or advance DQS signal to match the module-level clock signal CK with DQ(IN) and DQ(OUT)*, as reflected in in the figure below:



Ex. 2013 ¶ 112 (emphasis added) (with Figure 14A showing a timing chart at the time of starting write leveling and Figure 14B showing a timing chart at the end of leveling. (Ex. 1005 ¶ 27)).

The weight of the evidence disfavors Petitioner. We do not discern that Hiraishi discloses that the result of write leveling is used to affect the

data signals in the separate re-timing step, and Petitioner does not direct us to any portion in Hiraishi stating that. Instead, we are persuaded by Patent Owner's arguments, supported by expert testimony and Hiraishi's disclosures, discussed above, that write leveling is a part of the initialization operation, which is separate from the writing operation. Dr. Wedig acknowledged that the leveling processes occurs during the initializing period. *See* Ex. 2012, 57:3–10.

As discussed above, the evidence of record supports that Hiraishi's S4 write leveling is used to align the output DQS signal to the system clock signal CK. Dr. Wedig testifies that the *delays of S-4 write leveling are stored* in the data register buffer 300 *and then applied to delay* both the data and data strobe signals during subsequent write operations. Ex. 1003 ¶ 160 (emphasis added). But in light of the evidence that Hiraishi's S4 write leveling is used for aligning the DQS and CK signals, we do not discern why we should not credit Dr. Mangione-Smith's testimony, reproduced above, that the reason that Hiraishi's write leveling is stored, not to the delay data and strobe signals during subsequent write operations as Dr. Wedig testifies, but rather it is stored to be used to delay or advance the DQS signal to match the CK signal, in accordance with Dr. Mangione-Smith's testimony. Ex. 2013 ¶ 112. As noted, there was no expert testimony submitted with Petitioner's Reply to further address this issue. Accordingly, Dr. Mangione-Smith's testimony is not rebutted by other expert testimony. In view of Hiraishi's disclosures, we find Dr. Mangione-Smith's testimony on this issue to be credible, and we afford minimal weight to Dr. Wedig's conflicting testimony.

Additionally, in the Reply, Petitioner asserts that the rationale that the delays of S-4 write leveling would be stored in the data register buffer 300

and applied in the write (re-timing) in the two-step process, where S4 read/write leveling delays is used to determine a variable amount of delay, is "because data line L1 to the upper memory chip is longer than data line L2 to the lower memory chip." Pet. Reply 20–21 (citing Pet. 31–32; Ex. 1005 ¶¶ 55, 56, Fig. 1, Ex. 1074, 208:3–15, 210:24–211:22, 217:2–16, 223:20–224:4). At oral argument, Petitioner also referred to slide 24 (*see supra*, 52) for its support of assertions related to L1 and L2 and the two-step process, and the assertion that the write leveling delays are then used in the retiming process. Tr. 11:17–25, 12:9–13:4; *see also id.* at 9:17–10:15 (discussing "fork" in the L1 and L2 lines), 12:24–13:4 (discussing that "where first Hiraishi measures and stores the necessary delays as part of S4 read and write leveling," with a second step to address the different time delays for L1 and L2). We have reviewed the evidence presented by Petitioner on the L1/L2 issue, and we do not discern that the record provides support for its assertions on that issue. Instead, as discussed above, write leveling is used to address mismatches between the time of receipt of the clock signal CK and the data strobe signal DQS at memory chip 200, and not to account for delays in data signal lines.

Accordingly, considering the weight of the evidence, Petitioner does not carry its burden to demonstrate that Hiraishi teaches a two-step approach, with variable timing, where the result of write leveling is used to affect the data signals in the separate re-timing step.

We turn to Hiraishi's read leveling. In its Reply, Petitioner refers to the Petition at pages 48–51 for teachings on read leveling, and asserts that they are similar to those for write leveling. Pet. Reply 17. The Petition additionally contends that, with regard the read operation, (the alleged second step), Figure 11 of Hiraishi shows "the DQ/DQS read delays are

determined as the difference between the time of data output at CL=6 and time A of data arrival," which are based on "the timing of the control and clock signals (DRC, CK) carrying the read command (T0), the measured read data arrival time A from the memory, and a latency parameter (CL=6)." Pet. 49 (citing, *inter alia*, Ex. 1005 ¶¶ 163, 147–151, Fig. 11). Petitioner argues that the "delay circuitry delays the data and strobe signals (DQ/DQS) through the read data paths for subsequent read operations by an amount determined by the read leveling operation." *Id.*

We do not find that the evidence of record supports that the FIFO circuit 302, which Petitioner alleges is the "delay circuit," acts to "delay a signal through the data path" in Hiraishi's read leveling process. Figure 15 of Hiraishi is the timing chart for explaining the read leveling operation between the data register buffer and the memory chip. Ex. 1005 ¶ 28. Hiraishi describes the operation of read leveling shown in Figure 15 as:

> The read data DQ output from the memory chip 200 reaches the data register buffer 300, by which the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and *used in an adjustment of an activation timing of the input buffer circuit INB and the like*. In FIG. 15, two cases are shown including a first case that the time A from the input of the read command Read until the input of the read data DQ is short (between the memory chip 200-0 and the data register buffer 300-0) and a second case that the time A is long (between the memory chip 200-19 and the data register buffer 300-4).

Ex. 1005 ¶ 151 (emphasis added). As disclosed, Hiraishi's read leveling adjusts the activation timing of the input buffers and is not related to the FIFO. Dr. Wedig acknowledged the input and output tristate buffers were

not part of the delay circuit. Ex. 2012, 31:23–25[15]. Hiraishi further discloses that in read leveling "an output of read data DQ begins at the time T5. The read data DQ at the time of the read leveling is, for example, a signal in which a High level and a Low level are repeated in an alternate manner." Ex. 1005 ¶ 150. That is, Hiraishi's disclosures indicate that, in read leveling, the activation timing of the input buffer circuit is adjusted and signaling is done using alternate high and low levels, which indicates that the buffer is turned on and off at different times to affect the read leveling process. This has nothing to do with Hiraishi's FIFO. Thus, the evidence of record supports that Hiraishi's read leveling is not done by Petitioner's mapped "delay circuit," i.e., the FIFO.

Additionally, and relevant to both read and write leveling, Petitioner refers briefly to a MRS command as "the standard command initialization" in the Reply. Pet. Reply 17, n.3. At the oral hearing, Petitioner more specifically asserts that "Hiraishi teaches that S4 read/write leveling is performed (during initialization) in response to the MRS command, consistent with the JEDEC standard for DDR3." Ex. 1089, slide 38. We do not find that the evidence and argument provided by Petitioner sufficiently demonstrates that an MRS command, as disclosed in the JEDEC standard, is a command signal that one of skill in the art would use in Hiraishi. In slide 38 presented at oral hearing, Petitioner referred to testimony of Dr. Wedig, provided in support of the Petition. Ex. 1089, slide 38; Ex. 1003 ¶ 176 (*see*

[15] At the time of the Petition, Petitioner alleged that the "delay circuit" was a combination of the DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376. *See* Pet. 39. Accordingly, Dr. Wedig's testimony reflects that while the FIFO was part of the claimed "delay circuit," the tristate buffers were not.

fuller citation, *supra*, 55–56). Dr. Wedig's testimony states, in part, that a skilled artisan would have understood from Hiraishi's disclosure of the mode register setting step S3 followed by a leveling operations S4 (Ex. 1005 ¶¶ 139–140) that:

> the system memory controller instructs the command/address/control register buffer on Hiraishi's *module to perform the S4 read/write leveling using 'a first set of command signals,' similar to the mode switching commands and mode register set commands for read and write leveling in the memory devices. See, e.g., EX1020 (JESD79-3C)* at 31, 33, 48–54 (multi-purpose register for read calibration), 43 (mode register setting for write leveling).

Ex. 1003 ¶ 176 (emphasis added). First of all, as Petitioner shows in slide 38, the mode register setting occurs, not as part of the S4 read/write leveling, but rather as a separate earlier step (S3), so the S3 mode register setting step would not be relevant to S4 read/write leveling in Hiraishi. *See* Ex. 1005 ¶¶ 139–140; Fig. 13. Further, Dr. Wedig's testimony refers to the same disclosures on the S3 mode register setting step being followed by the S4 read/write leveling step as the predicate to form his opinion ("from this disclosure") "that S4 read/write leveling" "*is similar*" to the "mode register set commands and mode register set commands for read and write leveling," referencing JESD79-3C on read calibration and write leveling. *See* Ex. 1003 ¶ 176 (emphasis added). We do not find that the disclosure of an S3 mode register setting process step followed by a separate S4 read/write leveling process step would serve to motivate any "understanding" to look to other references concerning read and write leveling because, as discussed, the evidence supports that in Hiraishi S4 read and write leveling is a different step than S3 mode register setting step. Further, Dr. Wedig does not testify that an MRS command is used in Hiraishi; he only testifies that some other

unidentified "similar" command would be used in S4 read and write leveling. Thus, we do not find that the Hiraishi disclosures relied upon by Petitioner or Dr. Wedig's testimony supplant or undermine Hiraishi's explicit teachings on how its read and write leveling is done, as discussed above.

Additionally, in Reply, Petitioner refers to the assertion in the Petition that a person of skill "would have been motivated to implement Butt's data path controlling technique in Hiraishi's data register buffer." Pet. Reply 16 (citing Pet. 33–41; Ex. 1029, Figs. 2, 3; Ex. 1074, 181:19–183:1, 184:1–190:7, 199:2–200:2, 201:14–202:5; Ex. 1084, Figs. 2, 3, 14) (emphasis omitted). We have reviewed Petitioner's argument and evidence and do not find that it provides an explanation of how Butt's data path controlling techniques would be used in Hiraishi. For instance, the discussion in the Petition regarding limitation 1[f] simply repeats the general statement of the Reply. *See* Pet. 39–40 (citing Ex. 1003 ¶ 152; Ex. 1005, Fig. 5). We have reviewed Dr. Wedig's associated testimony and do not find that it provides explanations of how Butt's teachings would be used in Hiraishi, and, more specifically, in the two-step process of Hiraishi that Petitioner alleges. *See* Ex. 1003 ¶¶ 144–147, 152. Petitioner also cites to portions of testimony for Dr. Mangione-Smith's deposition testimony, where Petitioner's counsel walked though portions of Butt and another reference[16] with Dr. Mangione-Smith. *See* Ex. 1074, 181:19–183:1, 184:1–190:7, 199:2–200:2, 201:14–202:5. Dr. Mangione-Smith makes general statements in the deposition, but

[16] U.S. Patent 7,215,584 B2 (Ex. 1084), which is represented by Petitioner to be incorporated by reference into Butt. *See* Ex. 1074, 188:2–189:5 (citing Ex. 1029 ¶ 47).

there is no testimony or opinions offered concerning how Butt's teachings would be used in Hiraishi. *See id*.

Thus, Petitioner has not met its burden to demonstrate how the combination of Hiraishi and Butt teaches the limitations of claim 1.

Accordingly, on the entire record, Petitioner has not shown by a preponderance of the evidence that claim 1 is unpatentable over the combination of Hiraishi and Butt.

ii. Claims 2–5

By virtue of their dependency from independent claim 1, the challenges to dependent claims 2–5 based on the combination of Hiraishi and Butt do not demonstrate obviousness for the reasons explained above.

Accordingly, on the entire record, Petitioner has not shown by a preponderance of the evidence that claims 2–5 are unpatentable over the combination of Hiraishi and Butt.

E. Asserted Obviousness of Claims 1–5 Over Hiraishi, Butt, and Tokuhiro

Petitioner contends that claims 1–5 would have been obvious over the combination of Hiraishi, Butt, and Tokuhiro. Pet. 72–108. The basis of this challenge is Petitioner's assertion is that Tokuhiro's read circuit DR-1 would be added to Hiraishi, as shown in annotated Figure 5 of Hiraishi, reproduced below. Pet. 89.

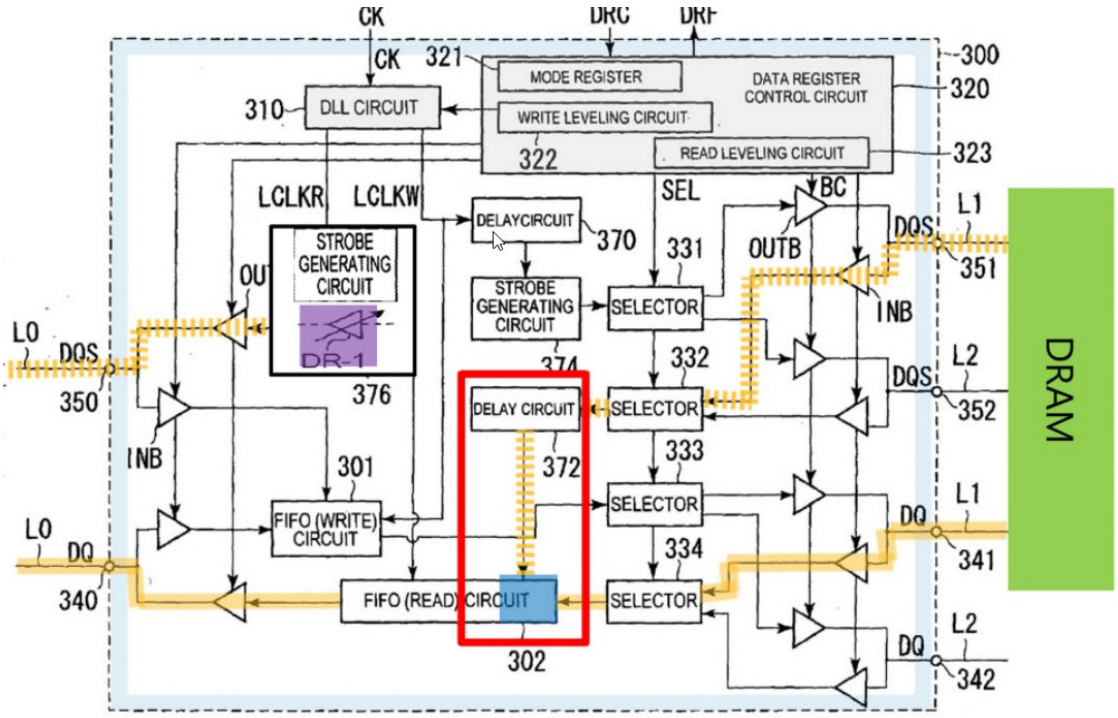


FIG.5

Annotated Figure 5, above, shows Tokuhiro's read circuit DR-1 added to a box containing Hiraishi's strobe generating circuit 376. Patent Owner argues that the combination of Hiraishi and Tokuhiro does not teach the claimed delay circuit in the data path. PO Resp. 58–59 (citing Ex. 2013 ¶¶ 91, 143–144). Dr. Mangione-Smith testifies that, in the combination, "the strobe generating circuit 376 is not in the DQ data path, nor is the DR-1 delay element which has been added to Hiraishi's buffer circuit." Ex. 2013 ¶ 144. In Reply, Petitioner contends that the asserted combination has a delay circuit in the data path because Patent Owner's arguments rely on the "erroneous claim constructions where the 'data path' excludes strobe signals, and the entire 'delay circuit' must be physically on top of the DQ data line." Pet. Reply 32–33 (emphasis omitted).

As we discussed above, claim 1 should be interpretated such that a "data path" corresponds to data signal lines that carry data signals, and not to

strobe signal lines that carry strobe signals. The data path that Petitioner relies upon in the combination of Hiraishi and Tokuhiro includes lines that carry strobe signals. Thus, Petitioner has not met its burden to demonstrate how the combination of Hiraishi, Butt, and Tokuhiro teaches the limitations of claim 1. By virtue of their dependency from independent claim 1, the challenges to dependent claims 2–5 also fail.

Accordingly, on the entire record, Petitioner has not shown by a preponderance of the evidence that claims 1–5 are unpatentable over the combination of Hiraishi, Butt, and Tokuhiro.

F. Asserted Obviousness of Claim 5 Over Hiraishi, Butt, and Ellsberry, with or without Tokuhiro

Petitioner relies on Ellsberry only for its teaching related to a claim limitation specific to claim 5, that is, memory devices having "*a data width of 4 bits*." Pet. 108–109. As such, Ellsberry does not cure the deficiencies of Petitioner's showing as to claim 1, as discussed above.

Thus, Petitioner has not met its burden to demonstrate how the combination of Hiraishi, Butt, and Ellsberry, with or without Tokuhiro teaches the limitations of claim 5.

Accordingly, on the entire record, Petitioner has not shown by a preponderance of the evidence that claim 5 is unpatentable over the combination of Hiraishi, Butt, and Ellsberry, with or without Tokuhiro.

III. MOTIONS

Petitioner filed a Motion to Exclude (Paper 31), with Patent Owner filing an Opposition (Paper 36), and Petitioner filing a Reply to the Opposition (Paper 38). In this Motion, Petitioner seeks to exclude Exhibit 2016, which is a transcript of a deposition of Dr. Wedig from another

proceeding. *See* Paper 31. We have not considered this evidence in this Decision, and therefore we *dismiss* the Motion to Exclude as moot.

Patent Owner filed a Motion to Strike (Paper 25), with Petitioner filing an Opposition (Paper 27). In this Motion, Patent Owner is seeking to strike portions of figures from pages 5, 10, 22, 27 (top figure), 28 (bottom figure), 30 (top figure), 39, 40, and 42 of Petitioner's Reply. Paper 25. Patent Owner's assertion is that Petitioner is attempting to circumvent the rules on word counts by excessive words in figures. *Id*. at 1 (citing 37 C.F.R. § 42.24(c)(1). Patent Owner also argues that, although Petitioner asserts that the blocks of text "simply mirror language already in the brief," the "words in the figures are framed differently and enable Petitioner to make additional arguments and elaborations using color coding and symbols." *Id*. at 4. Petitioner opposes the Motion because it contends that the descriptive annotations in the figures is helpful to the reader to "simply visualize written arguments already included in the word count," and Patent Owner does not dispute that the figures do not present new arguments. Paper 27.

As to the Motion to Strike, we agree with Patent Owner that Petitioner's addition of block quotes is extensive. *See*, e.g., Pet. Reply 22, 40, 42. We note, however, that the circumstances of this proceeding are atypical because, as discussed above, there were newly-raised arguments in Petitioner's Reply which we considered. Although Petitioner did not request additional words for its Reply, under these specific circumstances with the newly-raised argument in Reply, we allow the figures and the words in the figures to remain in the record. However, we agree with Patent Owner that the use of other annotations, such as color coding, symbols, and arrows could potentially be used as a way to reframe arguments. Thus, we strike

non-word annotations, such as color coding, symbols, and arrows, from Petitioner's Reply, to the extent that they were not already in documents previously in the record. A revised Petitioner's Reply, with annotations, such as color coding, symbols, and arrows, removed from the figures at issue shall be filed within 10 business days of the entry of this Judgment. According, we *grant-in-part* and *deny-in-part* Patent Owner's Motion to Strike.

Patent Owner filed a Motion to File Supplemental Information (Paper 35), with Petitioner filing an Opposition (Paper 37). We have not considered this evidence in this Decision, and therefore we *dismiss* the Motion to File Supplemental Information as moot.

IV. CONCLUSION

The outcome for the challenged claims of this Final Written Decision follows. In summary:

Claims	**35 U.S.C. §**	**References/ Basis**	**Claims Shown Unpatentable**	**Claims Not Shown Unpatentable**
1–5	103(a)	Hiraishi, Butt		1–5
1–5	103(a)	Hiraishi, Butt, Tokuhiro		1–5
5	103(a)	Hiraishi, Butt, Ellsberry		5
5	103(a)	Hiraishi, Butt, Tokuhiro, Ellsberry		5

Claims	35 U.S.C. §	References/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
Overall Outcome				1–5

V. ORDER

It is, therefore,

ORDERED that Petitioner has not demonstrated by a preponderance of the evidence that claims 1–5 of the '608 patent are unpatentable;

FURTHER ORDERED that Petitioner's Motion to Exclude is *dismissed* as moot;

FURTHER ORDERED that Patent Owner's Motion to Strike is *granted-in-part* and *denied-in-part*;

FURTHER ORDERED that a revised Petitioner's Reply, with annotations, such as color coding, symbols, and arrows, removed shall be filed within 10 business days of the entry of this Judgment;

FURTHER ORDERED that Patent Owner's Motion to Exclude is *dismissed* as moot; and

FURTHER ORDERED that because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2023-00847
Patent 10,268,608 B2

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